

ENGINEERING  
SPECIFICATION

SPEC 64709300

CD 4

REV L

DATE 2/7/79

PAGE 1 of 72

MEMORY PRODUCTS ENGINEERING DIVISION

## PRODUCT SPECIFICATION

FOR THE

FLAT-CABLE INTERFACE

STORAGE MODULE DRIVE FAMILY

SMD

RESPONSIBLE ORGANIZATION	ORIGINATOR	UNIT MANAGER	SECTION MANAGER	DEPARTMENT MANAGER
	<i>[Signature]</i> 10/5/76			
PRODUCT MANAGEMENT		<i>[Signature]</i> 10-05-76	<i>[Signature]</i> 10-05-76	<i>[Signature]</i>
OEM ENGINEERING		<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
DISK DRIVE DEVELOPMENT		<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i> 11/17/76
CONTROLLER DEVELOPMENT				
DISK SYSTEM DEVELOPMENT				
SOFTWARE DEVELOPMENT				
MEDIA DEVELOPMENT			<i>[Signature]</i> 10-8-76	
HEAD DEVELOPMENT			<i>[Signature]</i> 10-8-76	<i>[Signature]</i> 10/8/76
CIRCUIT DESIGN				

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 2

NORMANDALE OPERATIONS

## TABLE OF CONTENTS

	<u>Page</u>
1.0 SCOPE	4
2.0 APPLICABLE DOCUMENTS	4
3.0 GENERAL DESCRIPTION	4
3.1 Equipment Definition	4
3.2 Optional Configurations	8
3.3 Major Components	11
4.0 PERFORMANCE	12
4.1 Access-to-Data Characteristics	12
4.2 Data Capacity	14
4.3 Data Transfer Rate	15
4.4 Error Rates	15
4.5 Data Security	16
4.6 Stop Time	16
4.7 Start Time	16
5.0 RECORDING CHARACTERISTICS	17
5.1 Recording	17
5.2 Disk	17
5.3 Heads	17
5.4 Spindle	17
6.0 INTERFACE	19
6.1 Interface Definition	19
6.2 Signal Lines	29
6.3 Data Format and Data Control Timing	51
7.0 CONTROLS AND INDICATORS	57
7.1 Operator Panel	57
7.2 Maintenance Switch and Indicators	57
7.3 Channel Select and Reserve Switches and Indicators	58
7.4 Elapsed Time Meter	58
8.0 PHYSICAL SPECIFICATIONS	59
9.0 RELIABILITY AND SERVICE GOALS	59
9.1 Mean Time Between Failure	59
9.2 Mean Time to Repair	60
9.3 Preventive Maintenance Time	60
9.4 Service Life	60
10.0 INSTALLATION AND MAINTENANCE	60
10.1 Power Requirements	60
10.2 Grounding	65
10.3 Environmental Limits	65

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 3

NORMANDALE OPERATIONS

## ILLUSTRATION

<u>Figure</u>		<u>Page</u>
1	Major Component Placrmnt and Air Flow	6
2A	Basic SMD Styling Configurations	9
2B	Basic SMD Styling Configurations	10
3	SMD Maximum Seek Profile	13
4	Heads Viewed from Front of Machine	18
5	Block Diagram	20
6	Data Transmitter and Receiver	22
7	Control Line Transmitter	23
8	Control Line Receiver	24
9	Single and Dual Channel Interface	26
10A	9760/9762 I/O Panel	27
10B	9764/9766 I/O Panel	28
11A	Tag Bus I/O Interface	30
11B	"B" Cable Interface	31
11C	Tag Bus Decode	32
12	Tag and Bus Timing	33
13	Typical Timing with Address Mark	35
14	Index and Sector Timing	39
15A	Sample Priority Select Timing	42
15B	Logic Number Select and Timing Diagram	43
16	Seek End Timing	45
17A	9760/9762 Sequence Power Lines	47
17B	9764/9766 Sequence Power Lines	48
18	Data Timing	50
19A	Fixed Sector Format	52
19B	Variable Sector Format	53
20	Control Timing	56
21	Line Current Versus Start-Up Time	62
22	Input Power Connector	63
23	Input Power Connector	64
24	Vibration Levels	67
25A	9760/9762 Acoustic Cabinet Detail	68
25B	9760/9762 Acoustic Cabinet Detail, Drawer Mount SMD	69
26	9760/9762 Pedestal Cabinet Mount Detail	70
27	9764/9766 Acoustic Cabinet Detail	71
28	Desk Mount	72

## Tables

1	Accessories List	7
2A	I/O Cable Length and Tabs	19
2B	Shielded I/O Cable Length and Tabs	19
3	Physical Specifications	59
4	Primary Voltage Requirements	61
5	Primary Voltage Requirements	61

# ENGINEERING SPECIFICATION

SPEC 64709300

CD 4

REV

DATE

PAGE 4

NORMANDALE OPERATIONS

## 1.0 SCOPE

This document describes the MAGNETIC PERIPHERALS INC. Storage Module Drive {SMD} and its available configurations.

## 2.0 APPLICABLE DOCUMENTS

SPEC 70439600 - 9876 Disk Pack Product Specification {9760 SMD}  
SPEC 70438100 - 9877 Disk Pack Product Specification {9762 SMD}  
SPEC 70429600 - 9833-91 Disk Pack Product Specification  
                  {9764/9766 SMD}  
SPEC 64028500 - 9960 {TB304A} Field Test Unit  
STD UL 478 - Electronic Data Processing Units and Systems  
                  {60 Hz Units}  
CSA C22.2 - Canadian Standards Association, C22.2 No.154-1975  
                  Data Processing Equipment {60 Hz}  
DWG 77459200 - SMD Mechanical Interface  
PUBL 83322150 - Maintenance Manual Volume I 9760/9762  
PUBL 83322200 - Reference Manual 9760/9762  
PUBL 83322250 - Maintenance Manual Volume II 9760  
PUBL 83322240 - Maintenance Manual Volume II 9762  
PUBL 83322310 - Maintenance Manual 9764/9766  
PUBL 83322320 - Reference Manual 9764/9766  
PUBL 83322440 - CDC Microcircuits

## 3.0 GENERAL DESCRIPTION

### 3.1 Equipment Definition

The SMD is a 3600 rpm, 9.677 MHz data rate, random-access, mass memory device consisting of a disk pack spindle, drive motor and brake; a voice coil positioner and servo; a logic chassis with read/write, fault, and transmitter/receiver electronics; an air supply and filter; and a dc power supply. Available configurations are tabulated on the following page.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 5

NORMANDALE OPERATIONS

CONFIGURATION		STORAGE CAPACITY			
Power Requirements					
Voltage {V ac}	Frequency {Hz}	40 MB {9760, BK4XXX}	80 MB {9762, BK5XXX}	150 MB {9764, BK6XXX}	300 MB {9766, BK7XXX}
100	60	X	X		
120	60	X	X		
200/208/230	60			X	X
100	50	X	X		
200	50			X	X
220/240	50	X	X	X	X
Pedestal Cabinet		X	X		
Acoustic Cabinet		X	X	X	X
Drawer Mount		X	X		
Rack Mount 30 inches		X	X		
Rack Mount 36 inches		X	X		
Desk Mount		X	X		
Pack Access Cover Interlock		X	X	X	X
Index and Sector In "B" Cable		X	X	X	X

T18A

Several features to enhance system integrity are included as standard. They are phase-locked data separation, NRZ-to-MFM data conversion, variable sector {address mark}, and daisy-chain interface capability. These are defined in detail in this specification.

A hinged shroud cover on top of the SMD allows access to the spindle for pack installation and removal. A separate hinged enclosure cover provides access to the electronics, heads, and actuator, to perform maintenance procedures {on the 40/80 MB this cover has a lock to prevent access by unauthorized personnel}. Various electrical and mechanical options are available to the user to select the optimum configuration to best satisfy his individual system requirements. These options are described in 3.2.

Figure 1 illustrates the placement of the major components and the air flow through the device. Table 1 lists required accessories.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 6

NORMANDALE OPERATIONS

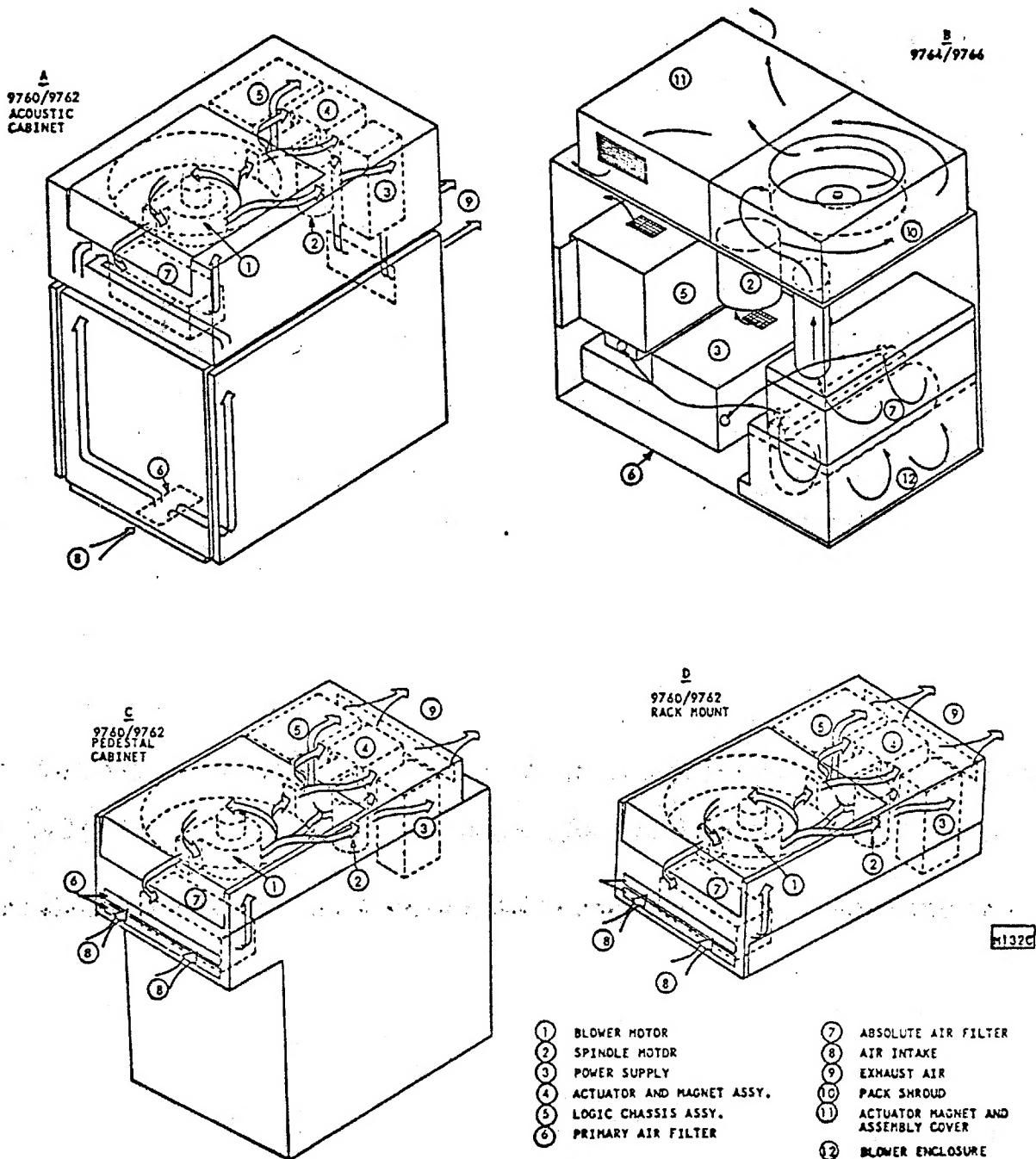


FIGURE 1. MAJOR COMPONENT PLACEMENT AND AIR FLOW

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 7

NORMANDALE OPERATIONS

TABLE 1. ACCESSORIES LIST

DESCRIPTION	QUANTITY REQUIRED	NOTE	PART NO.
"A" Cable {Controller to SMD}	One per SMD in star, one per multi-spindle installation in Daisy Chain	2,3,5	775642XX
"B" Cable {Controller to SMD}	One per SMD	3,5	775643XX
Logic Plug	One per SMD	1	943724XX
Terminator	One per SMD in star, one per multi-spindle installation in Daisy Chain	5	75841300
9876 Disk Pack for 9760	At least one per spindle		70439501
876-51 CE Disk Pack for 9760	Note 4		70439001
9877 Disk Pack for 9762	At least one per spindle		70438001
877-51 CE Disk Pack for 9762	Note 4		70438700
9883-91 Disk Pack for 9764/9766	At least one per spindle		70430514
883-51 CE Disk Pack for 9764/9766	Note 4		70430003
996{TB304-B} Field Exerciser	Note 4, 6		77449301
Head Alignment Kit	Note 4		77440503

1. Last two digits denote lens tab, one set {0 through 15} is provided with each SMD.
2. Multiple, number of cables required depends on number of units in daisy chain.
3. Last two digits denote length. {For cable length see Table 2.}
4. Quantity as required for regional maintenance.
5. In systems using the dual channel option, twice the number of cables and terminators are required.
6. Includes head alignment capability.

The above accessories {except for the logic plugs} are required but not included with the units; they must be purchased separately.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 8

NORMANDALE OPERATIONS

## 3.2 Optional Configurations

### 3.2.1 Optional Cabinetry and Power

#### 3.2.1.1 Pedestal Cabinet

The 40/80 MB devices are available in the pedestal cabinet (see Figures 2A(A) and 2B). Space for mounting a controller, etc., is available in the cabinet base.

#### 3.2.1.2 Acoustic Cabinet

The 40/80 MB devices are available in a desk height acoustic cabinet (see Figures 2A(B), 25A and 25B). Space for mounting a controller, etc., is available in the cabinet base.

The 150/300 MB SMDs are available only in the acoustic cabinet (see Figure 27).

#### 3.2.1.3 Drawer Mount

The 40/80 MB SMDs are available as a drawer mount which allows the customer to configure a 2 X SMD by placing it in the acoustic base cabinet. Hardware, slides, ballast weight and filler panels are included (see Figures 2A(C) and 25B).

#### 3.2.1.4 Rack Mount

A rack mount 40/80 MB SMD is available. The unit has slides, lock mechanism, and hardware necessary for mounting. (See Figures 28(D) and 28(E)). For rack mounting details and required clearances, see DWG 77459200.

#### 3.2.1.5 Desk Top

The 40/80 MB SMDs are available in a desk top cabinet (see Figures 28(F) and 28).

#### 3.2.1.6 Optional Power

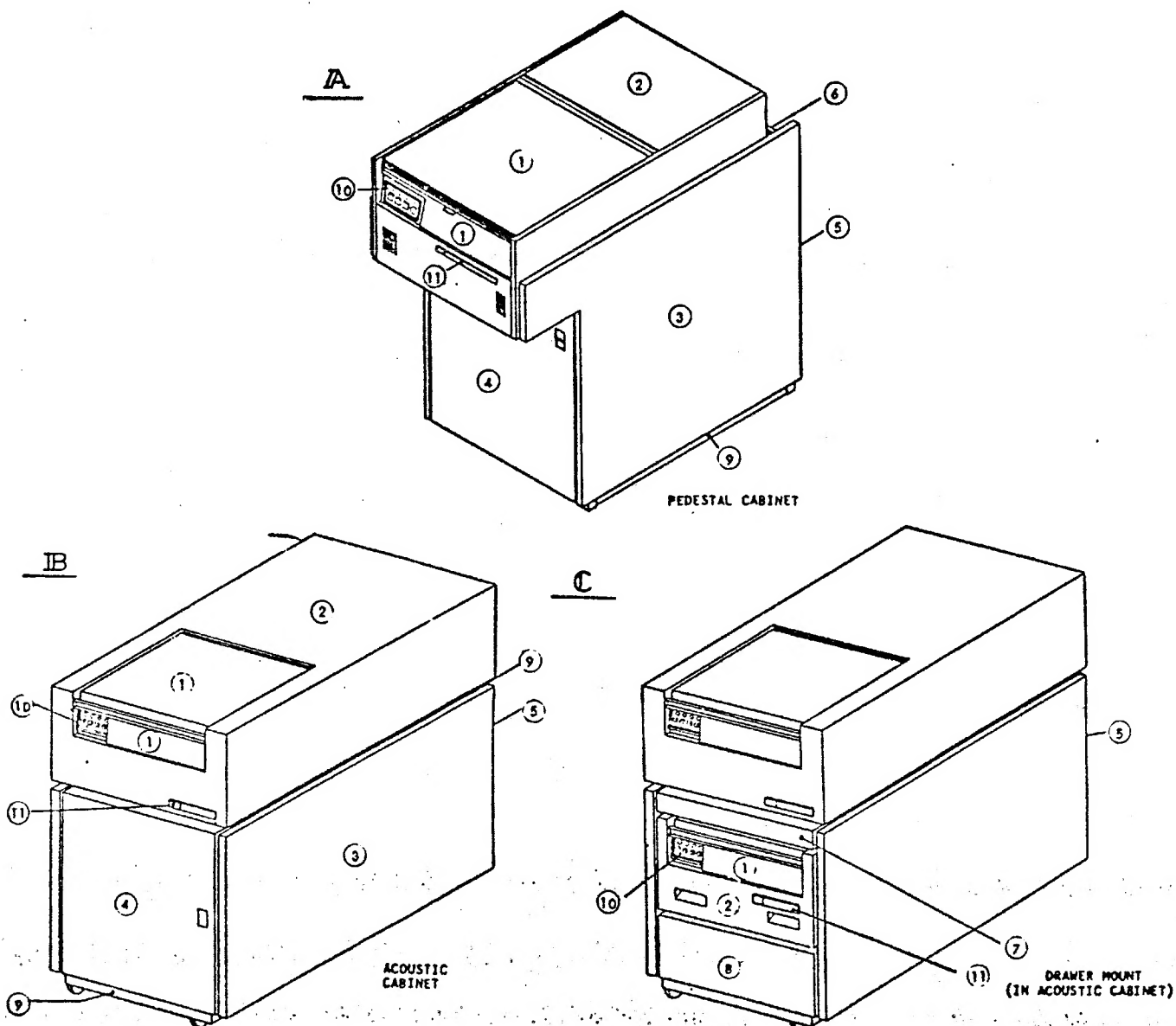
The 40/80 MB SMD is available for input power of 100 V ac, 50/60 Hz; 120 V ac, 60 Hz; or 220/240 V ac, 50 Hz single phase operation. The 150/300 MB SMD is available for input power of 200/208/230 V ac, 60 Hz; 200 V ac, 50 Hz; or 220/240 V ac, 50 Hz single phase operation.



# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 9

NORMANDALE OPERATIONS



FIND	ITEM NAME	BASIC CABINET A	ACOUSTIC CABINET B	DWR MOUNT IN ACOUSTIC CABINET C	CUSTOMER OPTION
1	PACK ACCESS COVER	IMPERIAL BLUE	IMPERIAL BLUE	IMPERIAL BLUE	YES
2	CASE	LIGHT GREY	LIGHT GREY	LIGHT GREY	YES
3	SIDE PANEL	LIGHT GREY	LIGHT GREY	-----	YES
4	FRONT DOOR	GREY BLACK	IMPERIAL BLUE	-----	YES
5	REAR DR (NOT SHOWN)	GREY BLACK	IMPERIAL BLUE	IMPERIAL BLUE	YES
6	FILLER STRIP	LIGHT GREY	-----	-----	YES
7	UPPER FRONT PANEL	-----	-----	LIGHT GREY	YES
8	LOWER FRONT PANEL	-----	-----	IMPERIAL BLUE	YES
9	FRAME AND BELTLINE	BLACK			NO
10	CONTROL PANEL	BLACK PHENOLIC			NO
11	PRODUCT EMBLEM	CDC PRODUCT IDENTIFICATION			YES

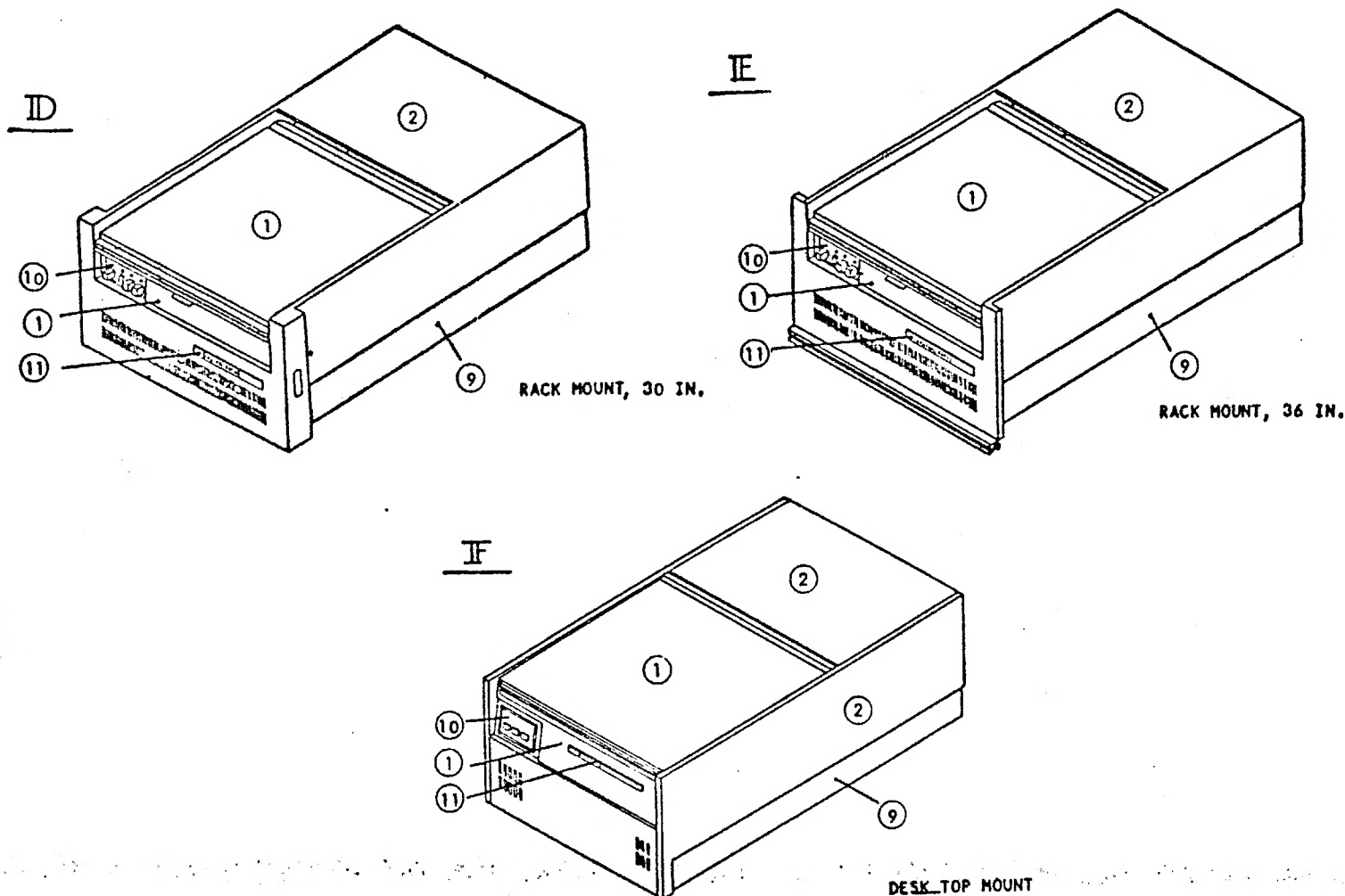
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FIGURE 2A. BASIC SMD STYLING CONFIGURATIONS

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 10

NORMANDEALE OPERATIONS



FIND	ITEM NAME	RACK MOUNT ID/E	DESK MOUNT IF	CUSTOMER OPTION
1	PACK ACCESS COVER	IMPERIAL BLUE	IMPERIAL BLUE	YES
2	CASE	LIGHT GREY	LIGHT GREY	YES
9	FRAME AND BELTLINE	BLACK		NO
10	CONTROL PANEL	BLACK PHENOLIC		NO
11	PRODUCT EMBLEM	CDC PRODUCT IDENTIFICATION		YES

F94A

FIGURE 2B. BASIC SMD STYLING CONFIGURATIONS

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 11

NORMANDALE OPERATIONS

## 3.2.2 Options

### 3.2.2.1 Pack Access Interlock Option

An interlock option is available that prevents the pack access cover from being opened until the pack has stopped spinning.

### 3.2.2.2 Index and Sector in "B" Cable Option

An option is available that places the index and sector pulses on the "B" cable (see Figure 11B).

### 3.2.2.3 Dual Channel Access Option

SMDs are available with dual channel access from the factory by special request. Single channel units are field upgradeable. The dual channel option allows two controller access of the SMD.

## 3.3 Major Components

### 3.3.1 Logic Assembly

The standard logic building blocks are dual-in-line TTL integrated circuits. ECL integrated circuits are used in critical read/write timing areas. The logic chassis is cooled by forced air (see Figure 1).

### 3.3.2 Positioner

Head positioning is performed by a closed-loop proportional servo system. The carriage is driven by a voice coil linear actuator with position feedback provided from the disk pack servo surface.

### 3.3.3 Deck and Spindle

A rigid, cast aluminum deck, spindle motor, and special spindle preserve the dimensional and speed integrity necessary for the recording system.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 12

NORMANDALE OPERATIONS

## 3.3.4 Air Supply

An air supply and filtering system is provided to meet the reliability requirements necessary for high density recording. Approximately 70 CFM for 9760/9762 {50 Hz}, 90 CFM for 9760/9762 {60 Hz}, 360 CFM for 9764/9766 {60 Hz}, or 300 CFM for 9764/9766 {50 Hz} of room air is moved through the unit to cool the disks, voice coil, and electronics.

For 9764/9766 SMDs, air enters the unit at the lower rear corner of cabinet, and it is discharged from the rear of the top cover.

For 9760/9762 SMDs, air is taken in through the front of the unit on the standard or rack mount SMD and in through the bottom on the acoustic or drawer mount SMD. The air is discharged through the rear.

## 3.3.5 Compatibility

The term "compatibility", when used in reference to the Magnetic Peripherals Inc. {MPI} family of 3600 rpm SMDs refers to disk pack interchangeability between spindles of any similar MPI 976X SMD. A disk pack written on an MPI 3600 rpm 976X SMD may be read on another similar MPI 3600 rpm 976X SMD {when using the same format} within the specified error rate.

## 4.0 PERFORMANCE

### 4.1 Access-to-Data Characteristics

#### 4.1.1 Positioning Times

All positioning times are measured from initiating a seek to the On Cylinder condition.

The maximum positioning time is 55 ms. This is defined as the time to move the head from track zero to track 822 {410 for 9760/9764}.

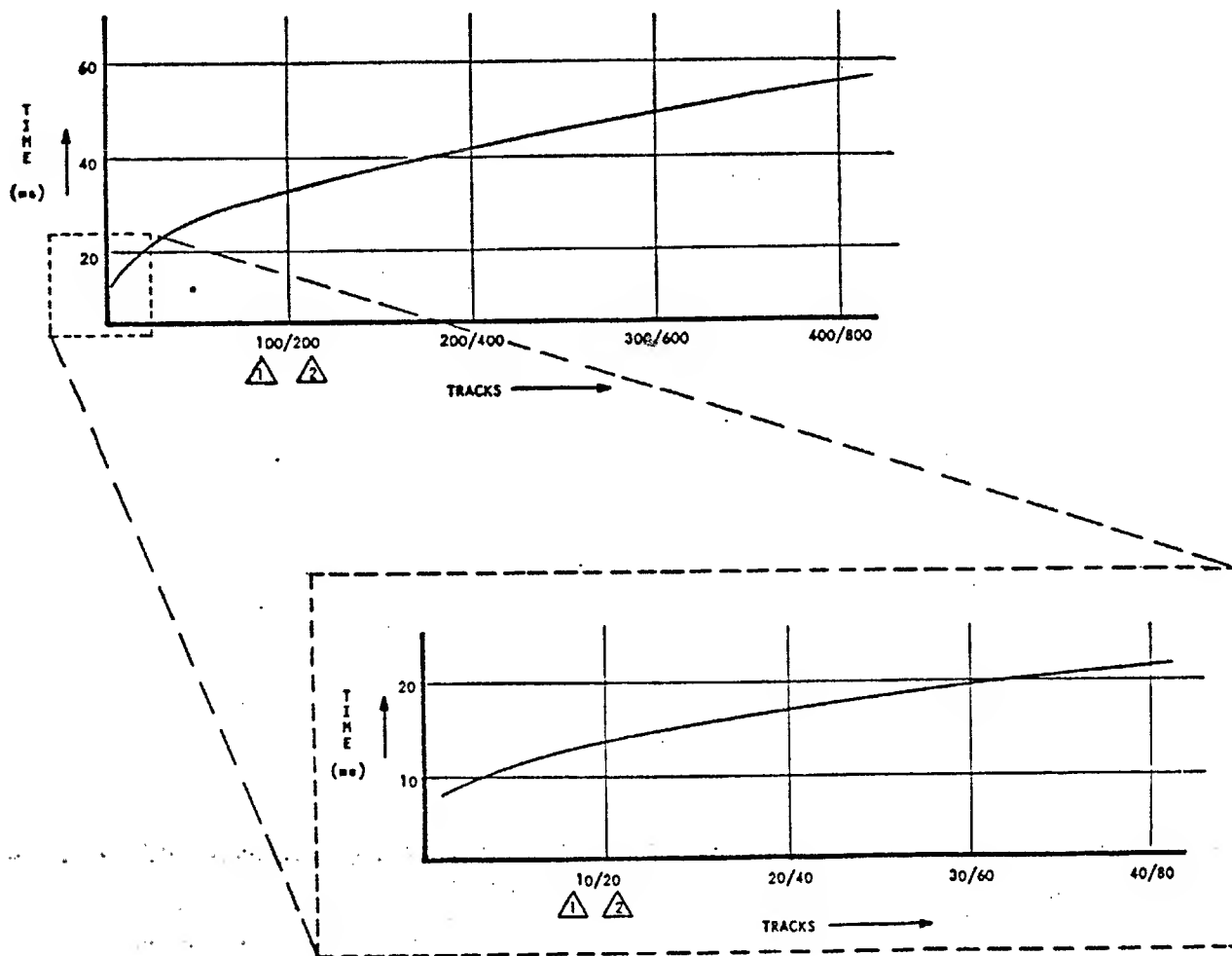
The maximum single track positioning time is 6 ms. This is defined as the time to move between any pair of adjacent tracks.

The average positioning time is no greater than 30 ms. This is defined as the time taken to make all possible moves divided by the number of all possible moves {see Figure 3}.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 13

NORMANDALE OPERATIONS



1 NUMBERS LOCATED ON LEFT SIDE OF THE DIAGONAL ARE APPLICABLE TO THE 9760 AND 9764, 192 TPI SMDs.

2 NUMBERS LOCATED ON RIGHT SIDE OF THE DIAGONAL ARE APPLICABLE TO THE 9762 AND 9766, 384 TPI SMDs.

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FIGURE 3. SMD MAXIMUM SEEK PROFILE

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 14

NORMANDALE OPERATIONS

## 4.1.2 Latency Time

The average latency time is 8.33 ms, based on a nominal disk speed of 3600 rpm.

The maximum latency time is 17.3 ms, based on a minimum disk speed of 3474 rpm {see 5.4}.

Latency time is defined as the time required to reach a particular track location after positioning is complete.

## 4.1.3 Read Initialization Time

Between the deselection of one head and the selection of another head, there is a 5.0  $\mu$ s delay within the SMD due to circuit characteristics. The time from the initiation of a head change until data can be read with a selected head without error, is 24.0  $\mu$ s, maximum {5.0  $\mu$ s for head selection, and 10  $\mu$ s for read amplifier stabilization and 9.0  $\mu$ s for phase lock synchronization}.

## 4.1.4 Write-to-Read Recovery Time

Assuming head selection is stabilized, the time lapse before read gate can be enabled after switching the write gate off is 10  $\mu$ s, minimum.

## 4.1.5 Read-to-Write Recovery Time

Assuming head selection is stabilized, the time lapse from dropping read gate to enabling write gate is 0.3  $\mu$ s, minimum {see Figures 18{A} and 18{B}}.

## 4.2 Data Capacity

The data capacity specified is based on the number of eight-bit bytes that are recorded on a track. The unsectored capacity below does not include an allowance for tolerance gaps.

DATA CAPACITY UNSECTORED	9760	9762	9764	9766
BYTES/TRACK	20 160	20 160	20 160	20 160
BYTES/CYLINDER	100 800	100 800	383 040	383 040
BYTES/SPINDLE {BASED ON 404/808 CYLINDERS}	40 723 200	81 446 400	154 748 160	309 496 320
CYLINDERS/UNIT	404 +7 SPARE	808 +15 SPARE	404 +7 SPARE	808 +15 SPARE

T46A

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 15

NORMANDALE OPERATIONS

## 4.3 Data Transfer Rate

The nominal bit rate is 9.677 MHz.

## 4.4 Error Rates {CDC Unit to CDC Unit}

The following error rates assume that the SMD is adjusted to specification, that the appropriate disk pack is being used, and the errors caused by media defects or equipment failures are excluded.

### 4.4.1 Read Errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

#### a. Recoverable Error Rate - 1 in $10^{10}$

The recoverable error rate is the number of errors encountered which are recoverable within three retries as a function of the number of bits transferred.

#### b. Unrecoverable Error Rate

An unrecoverable read error is one which cannot be read correctly within 27 retries {three retries at each combination of data strobe and carriage offset}.

Unrecoverable read errors shall be considered as failures affecting MTBF.

### 4.4.2 Write Errors

Write errors can occur as a result of the following: write data not being presented correctly, media defects, or equipment malfunction. As such, write errors are not predictable as a function of the number of bits passed.

For the case of an unrecoverable write error occurring because of a SMD equipment malfunction, the error is classified as a failure affecting MTBF.

Unrecoverable write errors are those which cannot be corrected within three attempts at writing and verifying the record.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 16

NORMANDALE OPERATIONS

## 4.4.3 Environmental Errors

When operating a low effective data transfer rate; e.g., random access of single short records, the effective error rate may be expected to exceed the above limits due to external environmental interference. The resulting recoverable read error rate is less than one error in eight hours of operation.

## 4.4.4 Access Errors

There is no more than one positioning error in  $10^6$  seeks.

## 4.5 Data Security

Under no circumstance of normal controller I/O operation is it possible to write a pattern not corresponding to that on the write data lines. It is possible to alter the bit pattern only when the SMD signifies an On Cylinder Status, and then only upon specific SMD selection. Data is protected by inhibiting Write Gate in all fault conditions including a loss of On Cylinder, Seek Error, or low voltage. Under any of the following conditions, an emergency retract of the heads is performed so that data is protected either by the above mentioned fault condition, or by switching off the voltage required to write.

1. Loss of ac line power.
2. Loss of speed.
3. Loss of  $\pm 5$ ,  $\pm 20$ , or  $\pm 42$ \* voltages.

\* $\pm 46$  V dc for 9764/9766

## 4.6 Stop Time

The time to stop a disk after the START/STOP switch has been turned off is 30 seconds, typical {35 seconds, maximum}. If power is lost, the spin-down time is 120 seconds, typical.

## 4.7 Start Time

The time for the SMD to be in the Ready state after the START/STOP switch has been depressed is 25 seconds, typical {35 seconds, maximum}.



# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 17

NORMANDALE OPERATIONS

## 5.0 RECORDING CHARACTERISTICS

### 5.1 Recording

Mode: MFM  
Density {inner track}: 6038 bpi nominal  
          {outer track}: 4038 bpi nominal

### 5.2 Disk {See Figure 4}

	<u>9760</u>	<u>9762</u>	<u>9764</u>	<u>9766</u>
Total number:	5	5	12	12
Cover disks:	2	2	2	2
Recording disks:	3	3	10	10
Servo surface:	1	1	1	1
Data surfaces:	5	5	19	19
Data tracks per surface:	404	808	404	808
Spares per surface:	7	15	7	15
Disk diameter in inches:	14	14	14	14
Track spacing in inches:	0.0052	0.0026	0.0052	0.0026
Tracks per inch:	192	384	192	384

### 5.3 Heads {See Figure 4}

	<u>9760</u>	<u>9762</u>	<u>9764</u>	<u>9766</u>
Servo head:	1	1	1	1
Recording heads:	5	5	19	19
Read/Write width in inches:	0.004	0.002	0.004	0.002
{No erase gap}				

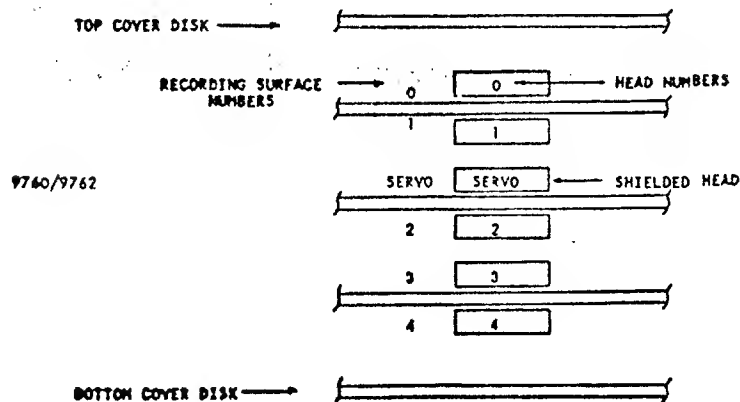
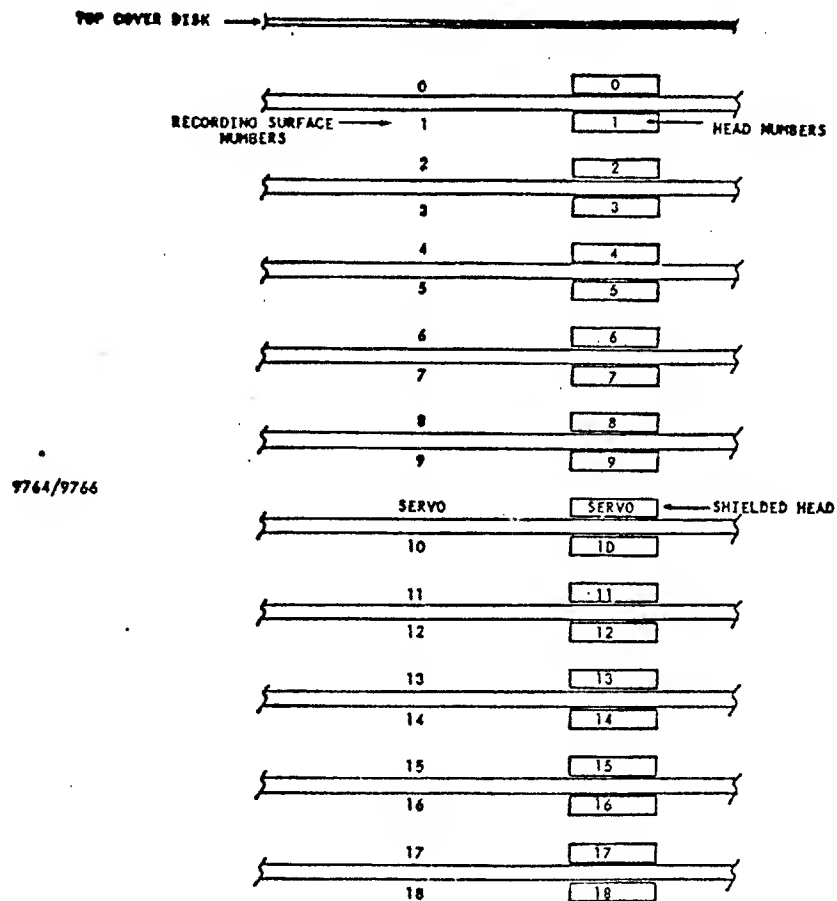
### 5.4 Spindle

The spindle speed is 3600 +90, -126 rpm. These limits represent +2.5% and -3.5% of nominal and are derived from motor performances, pulley tolerances and the mains power and frequency variations specified in 10.1.2, and 10.1.3.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 18

## NORMANDALE OPERATIONS



C84E

FIGURE 4. HEADS VIEWED FROM FRONT OF MACHINE

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 19

NORMANDALE OPERATIONS

## 6.0 INTERFACE

### 6.1 Interface Definition

The standard "A" cable I/O is 60 pin configuration. {See Tables 2A and 2B for I/O cable.}

All input and output signals are digital, utilizing industry standard transmitters and receivers to provide a terminated, balanced, transmission system for long distances and/or noisy electrical environment. Figure 5 is a block diagram of the SMD.

The "A" cable is a twisted-pair, flat cable. The "B" cable is a ribbon flat-cable with ground plane and drain wire, which allows mass termination without stripping. Twisted-pair and/or ground plane shielding is utilized to minimize cross-talk and reduce inductive coupling due to static discharges, as well as control impedance variations regardless of cable lay.

The I/O cables can also be made to satisfy UL requirements for over the floor cable by jacketing the cables.

TABLE 2A. I/O CABLE LENGTH AND TABS

	CABLE PART NUMBER TABS									
CABLE LENGTH IN FEET	5	6	8	10	15	20	25	30	40	50
"A" CABLE 775642XX	00	01	02	03	04	05	06	07	08	09
"B" CABLE 775643XX	00	01	02	03	04	05	06	07	08	09

TABLE 2B. SHIELDED I/O CABLE LENGTH AND TABS

	CABLE PART NUMBER TABS										
CABLE LENGTH IN FEET	4	5	6	8	10	15	20	25	30	40	50
60 PIN SHIELDED "A" CABLE 823724XX	10	00	01	02	03	04	05	06	07	08	09
26 PIN SHIELDED "B" CABLE 823659XX	NA	00	01	02	03	04	05	06	07	08	09

# ENGINEERING SPECIFICATION

NORMANDALE OPERATIONS

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 20

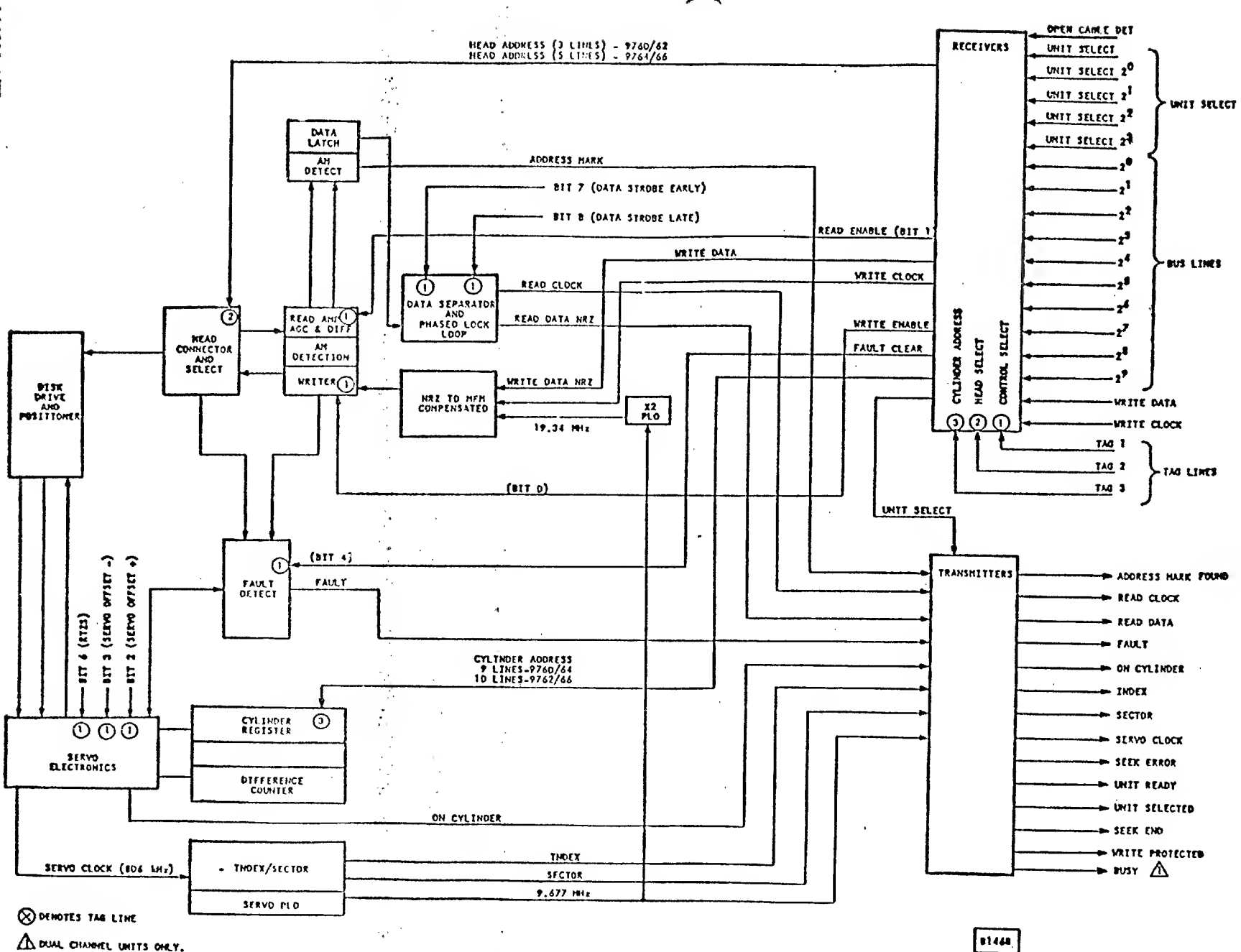


FIGURE 5. BLOCK DIAGRAM

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 21

NORMANDALE OPERATIONS

## 6.1.1 Terminated, Balanced Transmission System

Transmitters and receivers of the industry standard type 75110A and 75108 or equivalent are used to provide a terminated, balanced transmission system (see Figure 6).

## 6.1.2 Line Transmitter Characteristics

The SMD controller line transmitter (see Figure 7) is compatible with the CDC line receiver described in 6.1.3.

### 1. Output Signal Levels

- "A" Cable Control Signals - See Figure 7.
- "B" Cable Data Signals - See Figure 6.

### 2. Output Line Polarity

Control Signals - The CDC transmitter (see Figure 7) is connected to the I/O line such that the output, labeled Z, corresponds with the low order pin number of the pin assignments and in turn connect to receiver pin labeled B, except for the Unit Selected line, which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver.

## 6.1.3 Input Amplifier (Receiver) Characteristics

The SMD controller input amplifier (see Figure 8) is compatible with the CDC transmitter described in 6.1.2.

### 1. Receiver Propagation Delay

The receiver propagation delay is typically 17 ns in the direction of the logical 1, and 17 ns in the direction of the logical 0.

### 2. Receiver Input Polarity

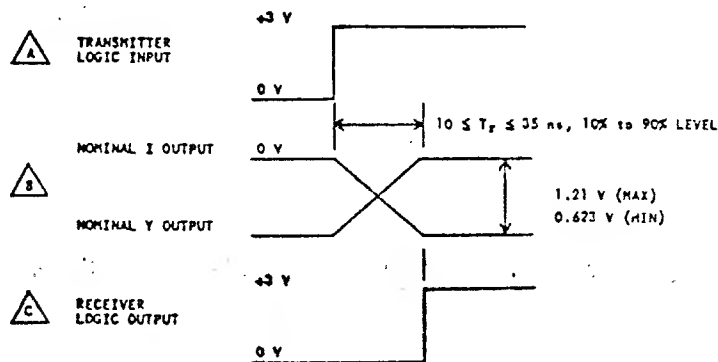
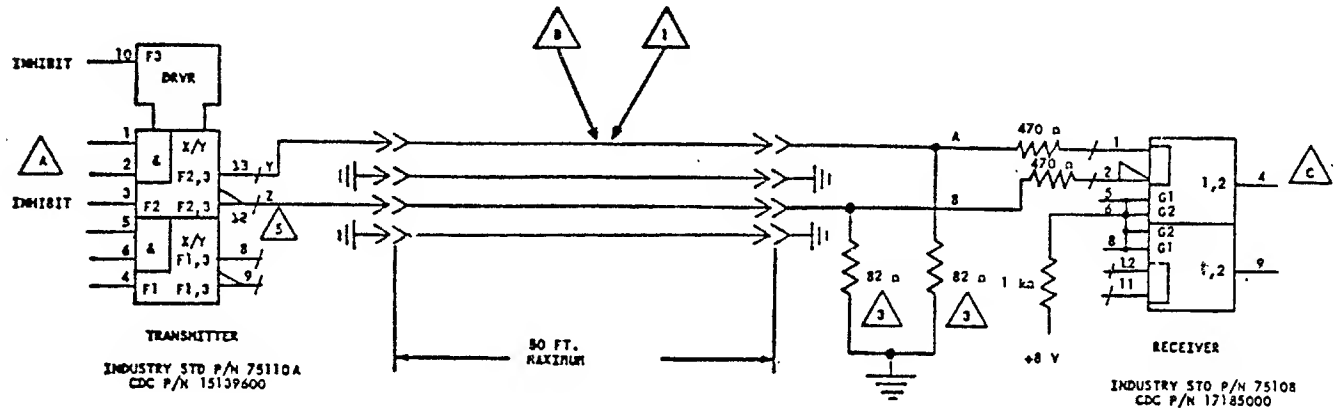
Control Signals - The input (labeled "B") of the receiver (see Figure 6) is connected to the lowest numbered pin of the pair in the cable and in turn connected to the transmitter pin labeled Z.

- "B" Cable Data Signals - See Figure 6.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 22

NORMANDALE OPERATIONS



- 1 CABLE IS FLAT CABLE WITH CHARACTERISTIC IMPEDANCE  $136 \pm 13$  OHMS, CDC P/N 775643 OR EQUIVALENT.
- 2 FOR LOGIC LEVELS AND TRUTH TABLE, REFER TO TRANSMITTER AND RECEIVER TEXT.
- 3 TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE STAR CABLED.

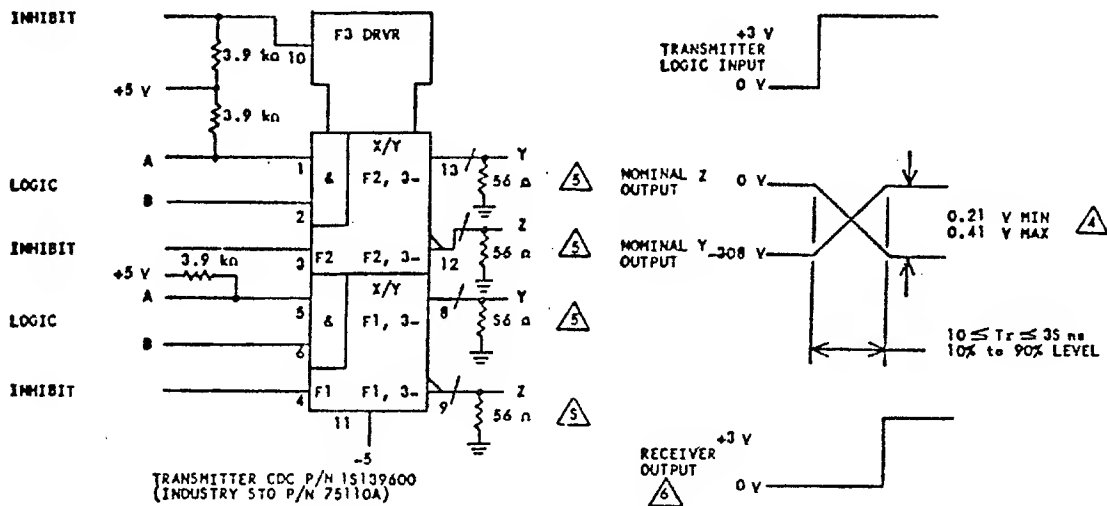
5140A



FIGURE 6. DATA TRANSMITTER AND RECEIVER

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 23

## NORMANDALE OPERATIONS



LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	F2	F1	Y	Z
L or H	L or H	L	L or H	H	
L or H	L or H	L or H	L	H	
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

## TRUTH TABLES

S105A

NOTES:

1. OUTPUT LEVELS - L = MOST NEGATIVE LEVEL  
H = LEAST NEGATIVE LEVEL

2. INPUT LEVELS - H = MOST POSITIVE LEVEL  
L = LEAST POSITIVE LEVEL

3 THIS IS AN INDETERMINATE INSTRUCTION WHEN SENSED BY AN ACTIVE (SELECTED) RECEIVER.

4 VOLTAGE RANGE INCLUDES TRANSMITTER OUTPUT SWING IN LOW STATE OF  $11 \pm 3$  mA, AND TERMINATING RESISTOR RANGE OF  $56 \pm 5\%$  OHMS.

5. TERMINATING RESISTORS ARE REQUIRED ON ALL "A" CABLE TRANSMITTERS. TRANSMITTERS IN THE DRIVE ARE TERMINATED BY THE TERMINATOR ASSEMBLY. REFER TO SINGLE AND DUAL CHANNEL INTERFACE ILLUSTRATION, AND THE TERMINATOR PARAGRAPH.

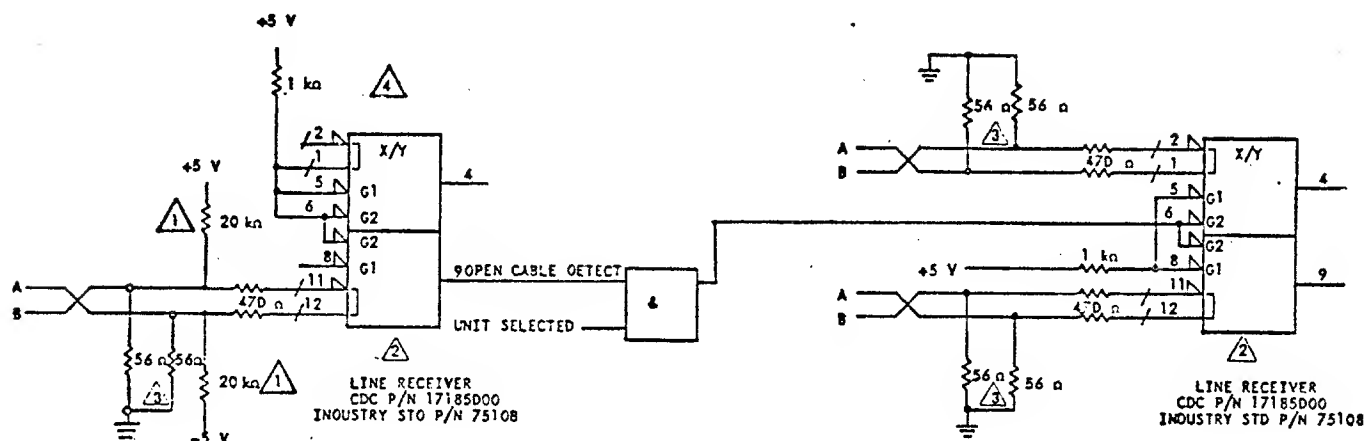
RECEIVER INPUTS A AND B ARE CONNECTED TO TRANSMITTER  
OUTPUTS Y AND Z RESPECTIVELY.

FIGURE 7. CONTROL LINE TRANSMITTER

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 24

NORMANDALE OPERATIONS



S1068

## NOTES:

1. 20 kΩ RESISTORS ARE TYPICAL VALUES.
2. A BIAS NETWORK SHOULD BE USED TO PREVENT FALSE STATUS OR INTERRUPT CONDITIONS WHEN DRIVE POWER IS OFF AT CONTROLLER END OF UNIT SELECTED AND SEEK END SIGNALS.
3. TERMINATING RESISTORS ARE LOCATED:  
A. ON LOGIC CARD FOR "B" CABLE LINES.  
B. IN SEPARATE TERMINATOR ASSEMBLY FOR "A" CABLE.
4. SEE 8.2.2.7 FOR DESCRIPTION OF OPEN CABLE DETECT SIGNAL.

DIFFERENTIAL INPUTS	INHIBIT		OUTPUT
	G1	G2	
$V_A - V_B \geq 25 \text{ mV}$	L or H	L or H	H
$ V_A - V_B  < 25 \text{ mV}$	L or H	L	H
	L	L or H	H
	H	H	IND.
$V_B - V_A \geq 25 \text{ mV}$	L or H	L	H
	L	L or H	H
	H	H	L

LINE RECEIVER TRUTH TABLE

FIGURE 8. CONTROL LINE RECEIVER



# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 25

NORMANDALE OPERATIONS

## b.1.4 Terminator

### 1. "A" Cable

A termination resistance as shown in Figures 7 and 8 is required at the transmitter and receiver end of each transmission line of the "A" cable. This resistance is provided on the unit by the terminator assembly (see Table 1 and Figure 9), which must be ordered separately (P/N 74841300).

A termination resistance is required at the controller end of each line of the "A" cable except for the Open Cable Detect line. See b.2.2(7). No termination resistance is used on the Power Sequence lines in the "A" cable.

### 2. "B" Cable

A termination resistance as shown in Figure 6 is required at the receiver end of each transmission line of the "B" cable. This resistance is provided at the unit's receiver logic card.

## b.1.5 I/O Connectors (See Figure 10A and 10B)

### b.1.5.1 "A" Cable Connector

DESCRIPTION	CDC P/N	BERG P/N	P/N SPECTRA-STRIP
Connector (60 pos.)	94361115	65043-007	-----
Flat cable (twisted-pair), 30 pair, 28 AWG	95043902	---	3CT-6028-78-05-100
Connector pins	94245603	48048	

### b.1.5.2 "A" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	CDC P/N	AMP P/N
60 pin, right angle header	94369804	3-86479-4
60 pin, vertical header	94385129	3-87227-0

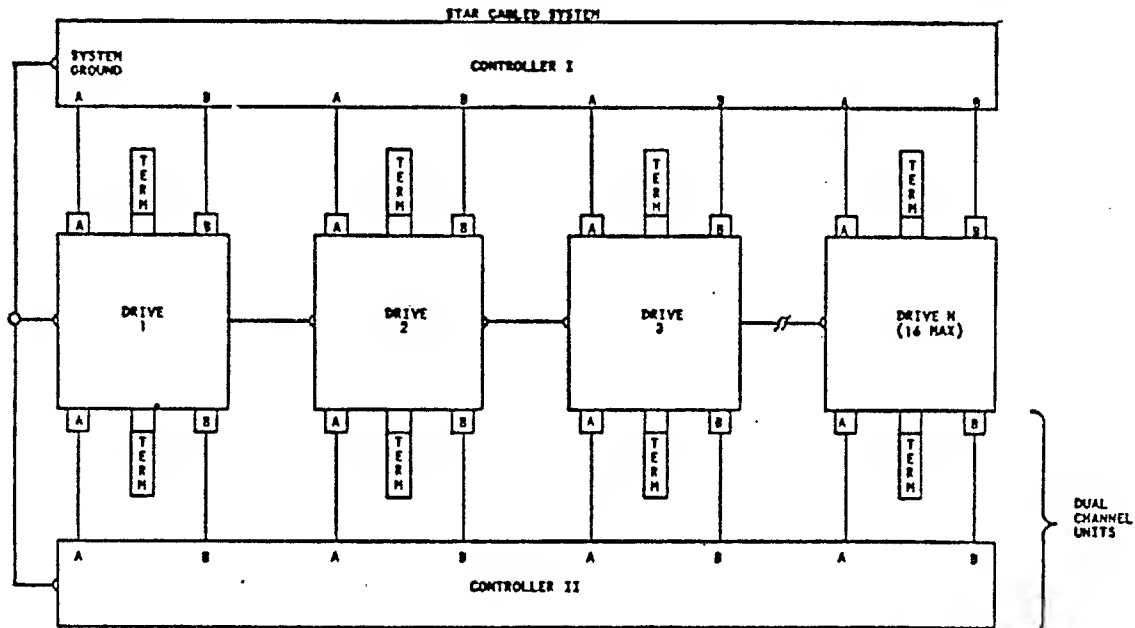
### b.1.5.3 "B" Cable Connector

DESCRIPTION	CDC P/N	3M P/N
Connector (26 pos.)	65853402	3399-3000
Connector pull tab	92004801	3490-2
Flat cable (26 pos.) with ground plane and drain wire. (Intra-cabinet only)	95028509	3476-26

# ENGINEERING SPECIFICATION

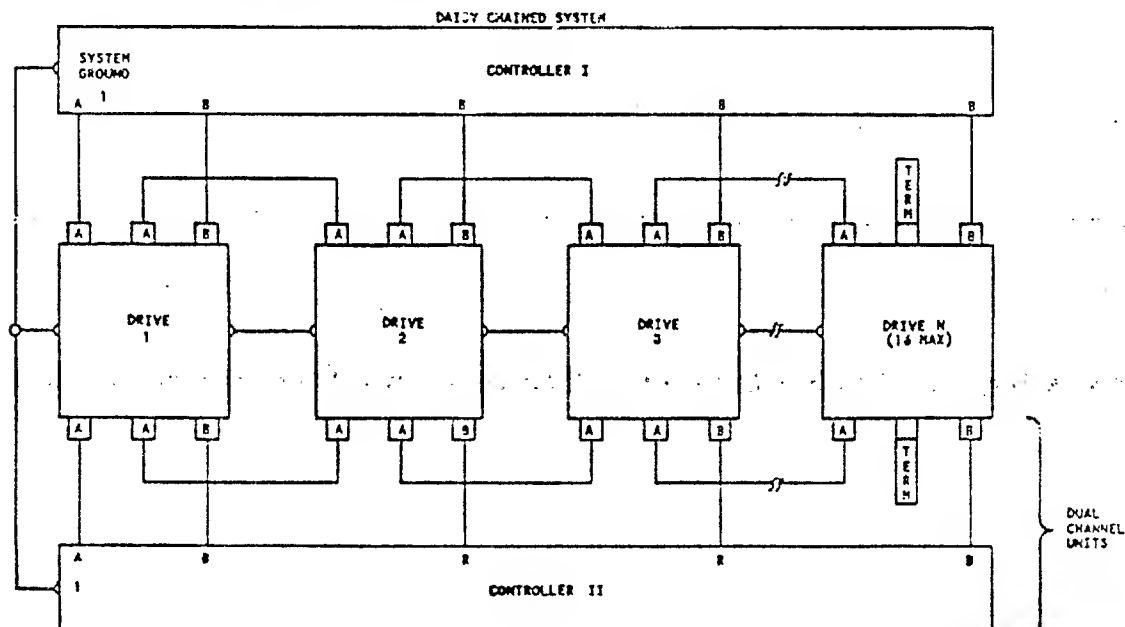
SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 26

## NORMANDEALE OPERATIONS



### NOTES

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET



### NOTES

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A STAR.
2. TERMINATION OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND ARE ON THE UNIT'S RECEIVER CARDS.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 100 FEET .  
 MAXIMUM INDIVIDUAL B CABLE LENGTH = 50 FEET.

21678

FIGURE 9. SINGLE AND DUAL CHANNEL INTERFACE

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 27

NORMANDALE OPERATIONS

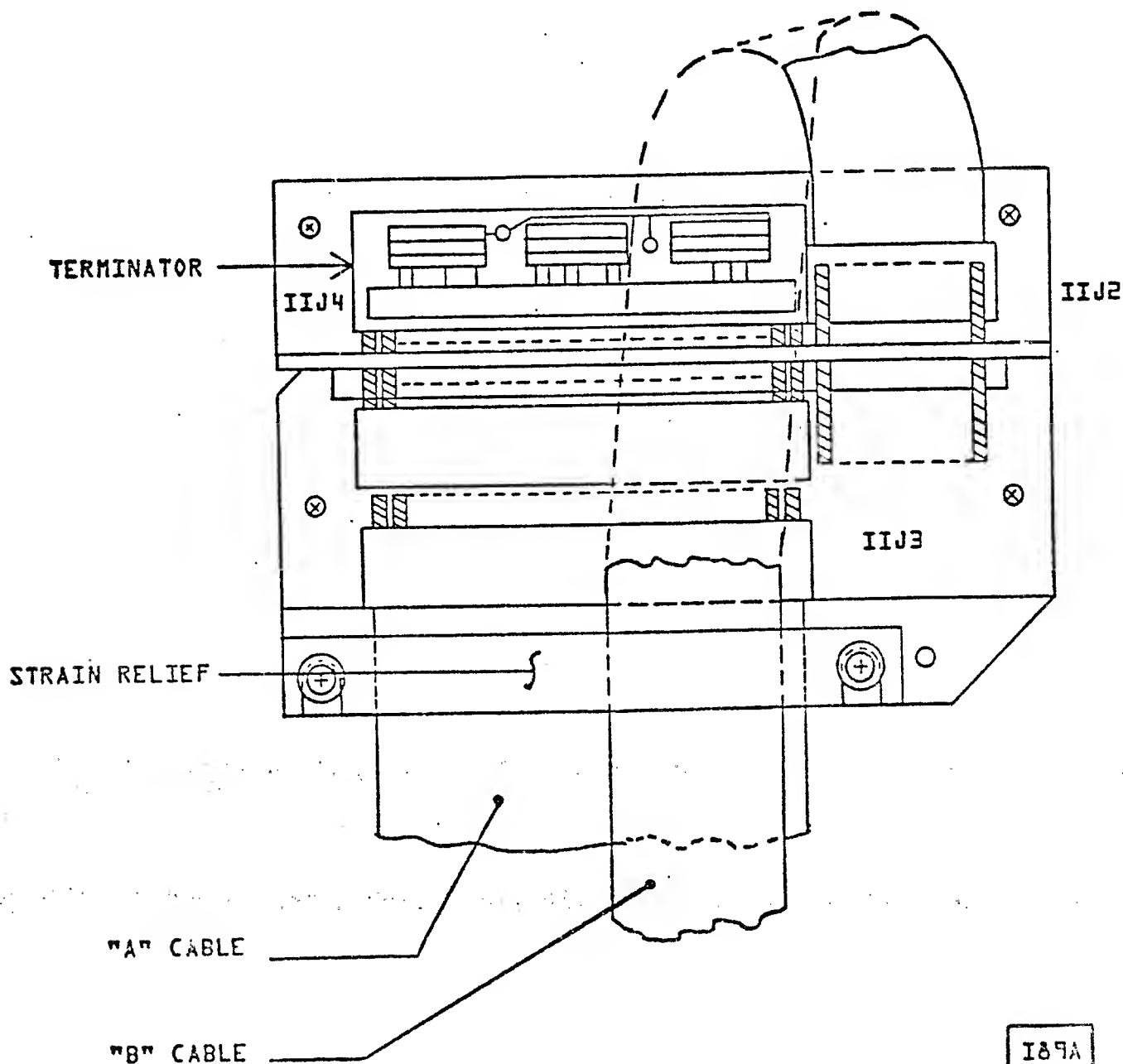
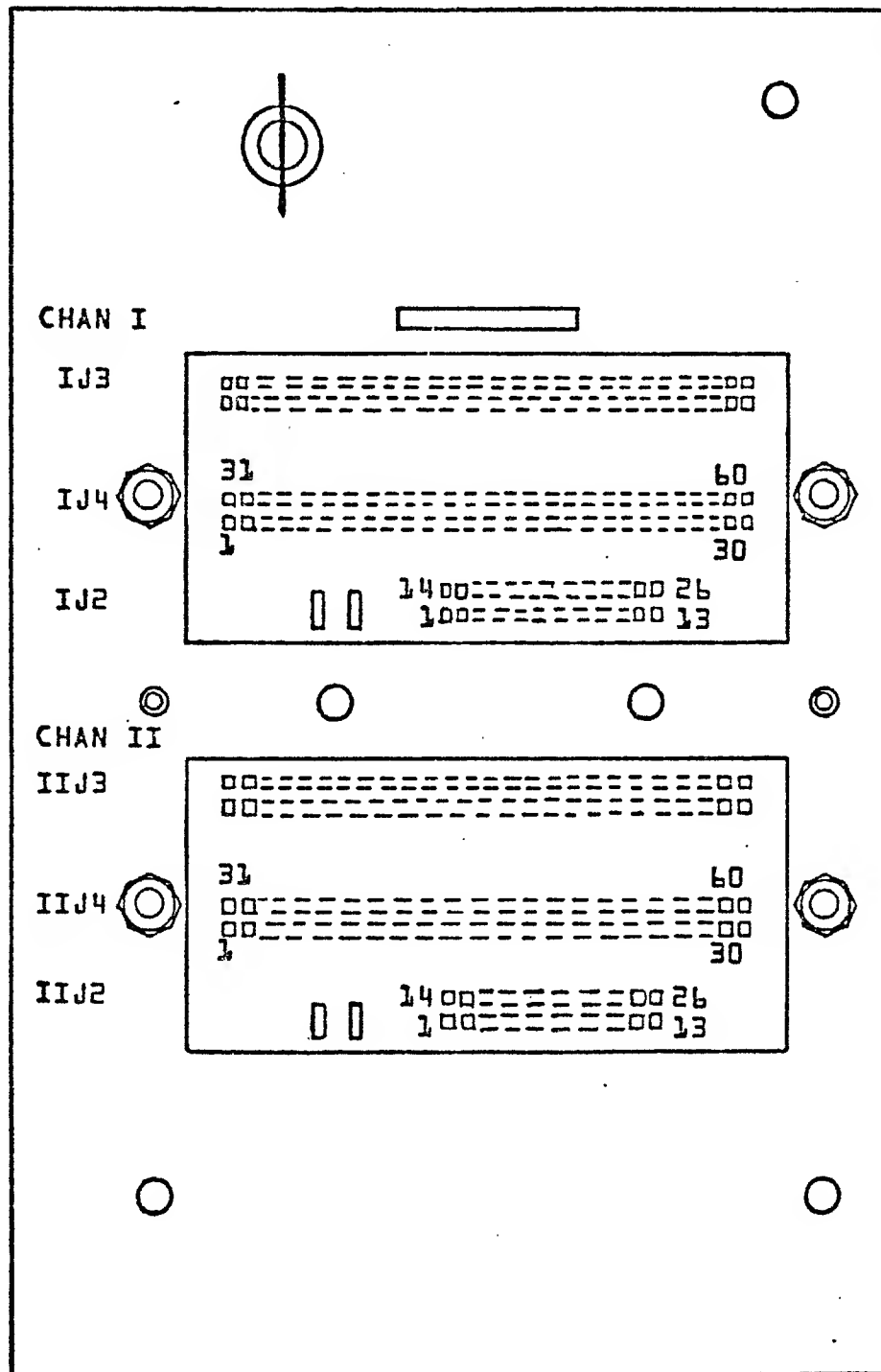


FIGURE 10A. 9760/9762 I/O CONNECTORS (PANEL)

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 28

NORMANDALE OPERATIONS



I90A

FIGURE 108. 9764/9766 I/O CONNECTORS (PANEL)

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 29

NORMANDALE OPERATIONS

## 6.1.5.4 "B" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	CDC P/N	AMP P/N
26 pin, right angle header	94369802	1-86479-0
26 pin, vertical header	94385106	1-87227-3

## 6.1.6 I/O Cable Characteristics

### "A" Cable

Type: 30 twisted pair, flat-cable  
Twist per inch: 2  
Impedance:  $100 \pm 10 \Omega$   
Wire size: 28 AWG, 7 strands  
Propagation time: 1.6 to 1.8 ns/ft  
Maximum cable length: 100 ft cumulative  
Voltage rating: 300 V rms

### "B" Cable {with ground plane}

Type: 26 conductor, flat cable with ground plane and drain wire  
Impedance:  $130 \pm 15 \Omega$  {3M P/N 3476/26}  
Wire size: No. 28 AWG - 7 strands  
Propagation time: 1.65 ns/ft  
Maximum cable length: 50 ft  
Voltage rating: 300 V rms

## 6.2 Signal Lines

Refer to Figure 11A for the "A" {Address/Control} cable and Figure 11B for the "B" {data} cable I/O signals.

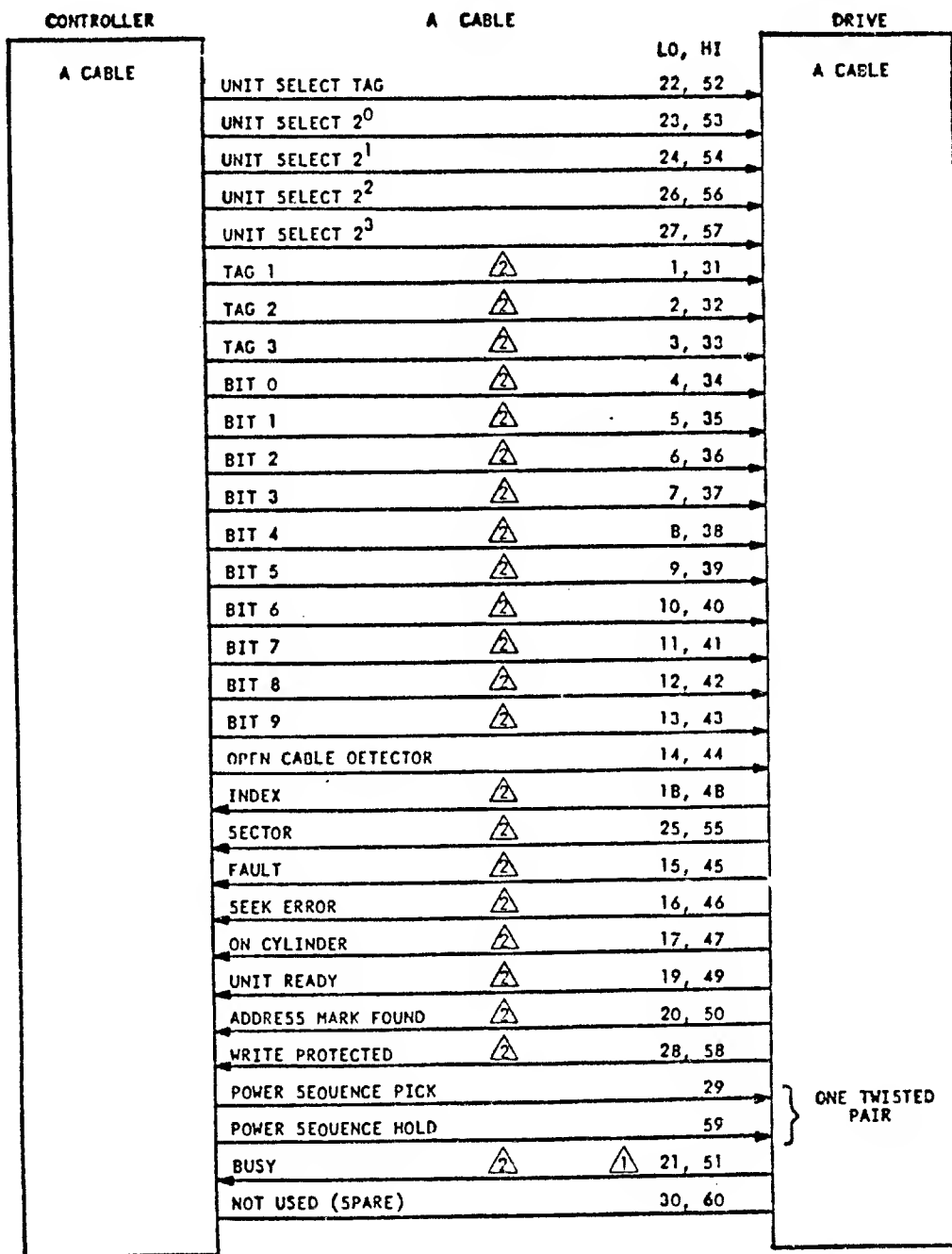
### 6.2.1 Address and Control Tag Functions

Address and Control functions are transferred on 10 lines. The significance of the information on these lines is indicated by one of three Tag Lines {see Figure 11C}. See Figure 12 for timing.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 30

NORMANDALE OPERATIONS



1125B

NOTE: 60 POSITION  
 28 AWG, 30 TWISTED PAIR - STRAIGHT FLAT CABLE  
 MAXIMUM LENGTH - 100 FT

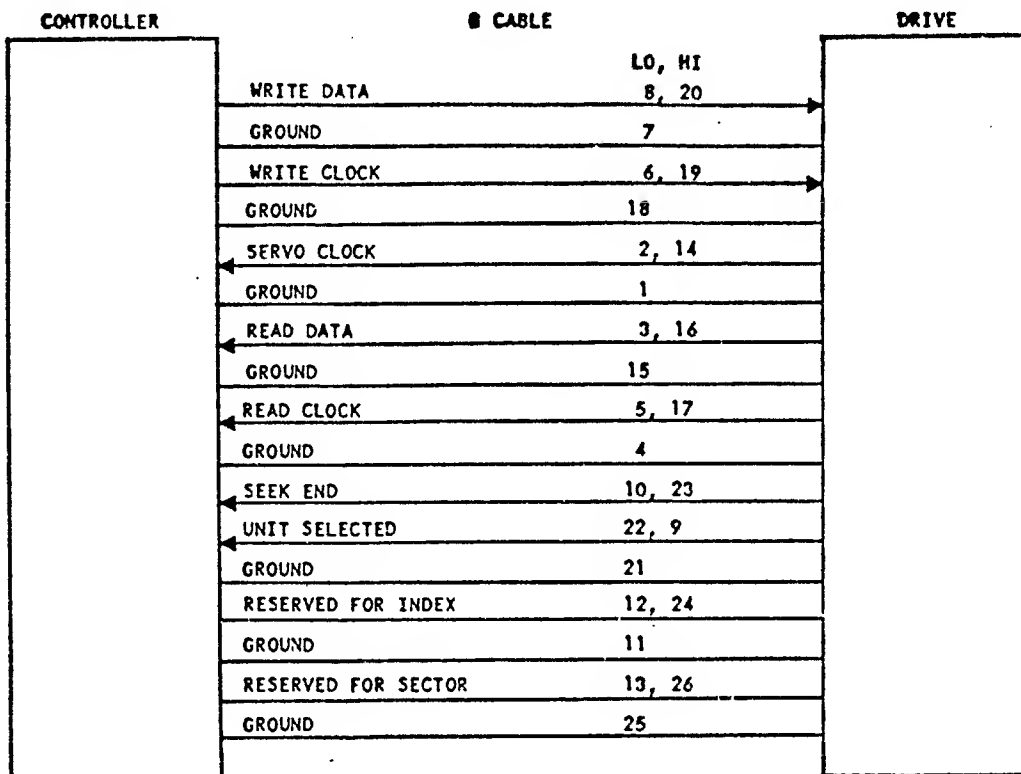
- △ DUAL CHANNEL UNITS ONLY.
- △ GATED BY UNIT SELECTED.

FIGURE 11A. TAG BUS I/O INTERFACE

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 31

NORMANDALE OPERATIONS



I88A

## NOTES:





1. 26 CONDUCTOR, FLAT CABLE MAXIMUM LENGTH - 50 FT
2. NO SIGNALS GATED BY UNIT SELECTED.


FIGURE 11B. "B" CABLE INTERFACE

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 32

NORMANDALE OPERATIONS

BUS	TAG 1 IN	TAG 2 IN	TAG 3 IN	UNIT SELECT
	CYLINDER ADDRESS	HEAD SELECT	CONTROL SELECT	
Bit 0	$2^0$	$2^0$	Write Gate	
1	$2^1$	$2^1$	Read Gate	
2	$2^2$	$2^2$	Servo Offset Plus	
3	$2^3$	$2^3$ 	Servo Offset Minus	
4	$2^4$	$2^4$ 	Fault Clear	
5	$2^5$		AM Enable	
6	$2^6$		RTZ	
7	$2^7$		Data Strobe Early	
8	$2^8$		Data Strobe Late	
9	$2^9$		Release 	Priority Select 

 FOR 9764/9766

 DUAL CHANNEL ONLY

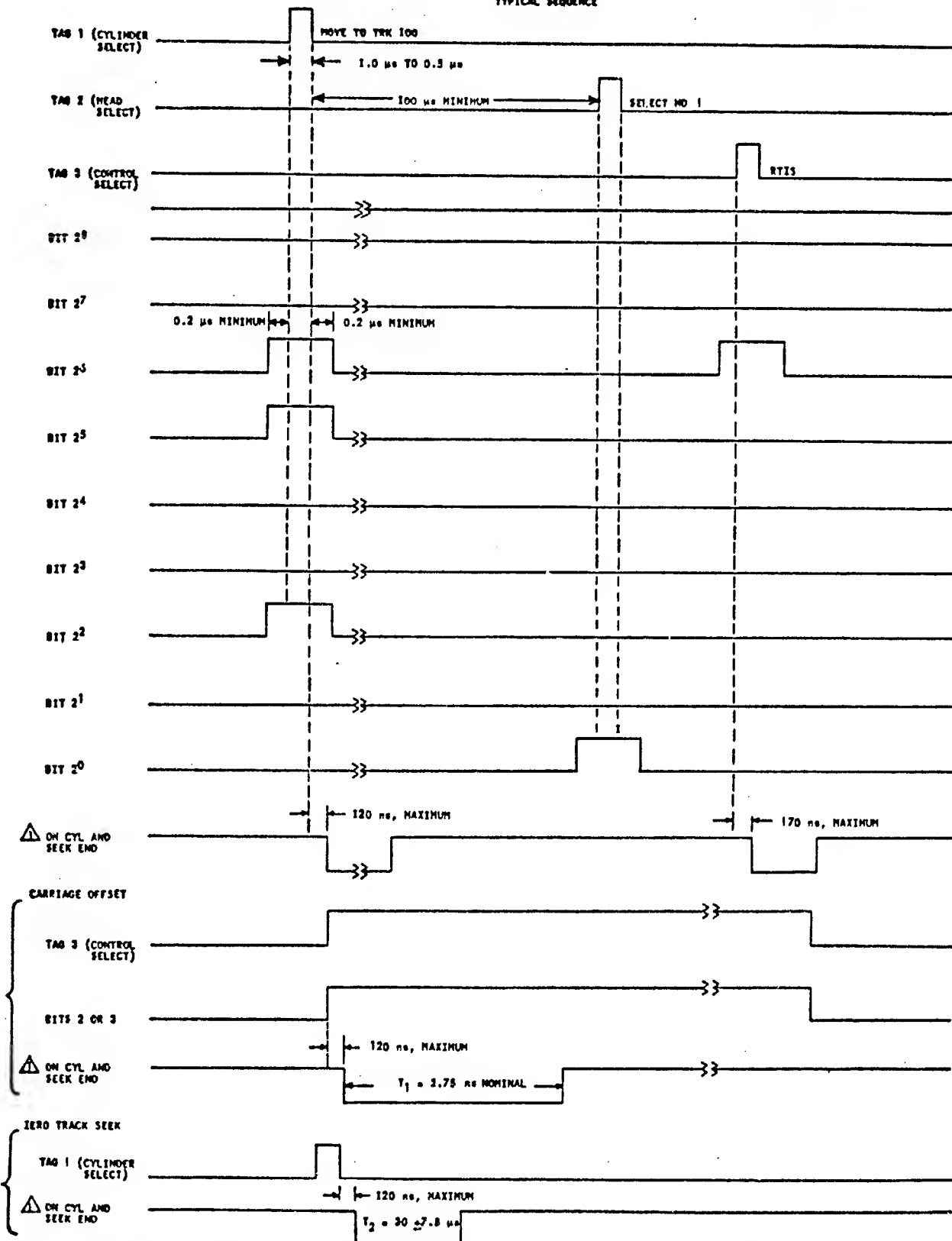
FIGURE 11C. TAG BUS DECODE



# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 33

## NORMANDALE OPERATIONS TYPICAL SEQUENCE



⚠ ON CYL AND SEEK END SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER. SEE NOTE ⚠.  
SEE 4.2.2(11).

FIGURE 12. TAG AND BUS TIMING

1208

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 34

NORMANDALE OPERATIONS

## 6.2.1.1 Cylinder Address {Tag 1}

The SMD is a direct addressing device, the controller need only place the new address on the Bus Lines and strobe the lines with Tag 1. The unit must be On Cylinder before Tag 1 is sent.

## 6.2.1.2 Head Select {Tag 2}

This signal is the head address that will be selected by bits 0 through 4 {see Figure 11C}. Head Select for the 9760/62 is 0 through 2 and for the 9764/66 it is 0 through 4.

## 6.2.1.3 Control Select {Tag 3}

This signal acts as an enable and must be true for the entire control operation.

### 1. Write Gate {Bit 0}

The Write Gate line enables the write drive {see Figure 11C}.

### 2. Read Gate {Bit 1}

Enabling of the Read Gate {see Figure 11C} enables digital read data to the transmission lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern {see Figure 13 for Read Gate and Write Splice relationship}.

### 3. Servo Offset Plus {Bit 2} See Note

When this signal is true, the actuator is offset from the nominal On Cylinder position towards the spindle.

### 4. Servo Offset Minus {Bit 3} See Note

When this signal is true, the actuator is offset from the nominal On Cylinder position away from the spindle.

### 5. Fault Clear {Bit 4}

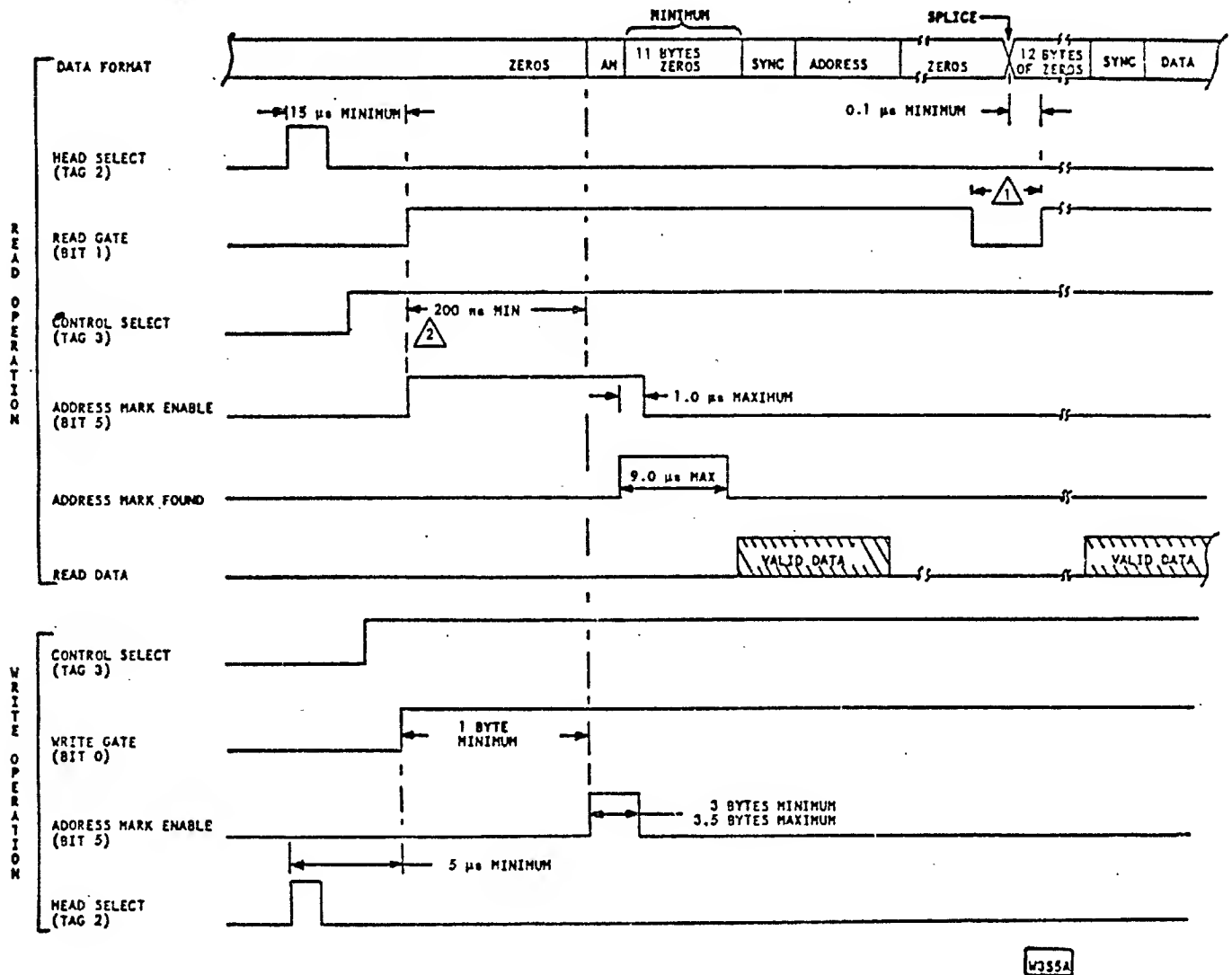
A 100 ns minimum pulse sent to the SMD will clear the fault flip-flop if the fault condition no longer exists.

NOTE: When dropping Offset Plus or Minus a 4 ms delay is required before a Read or Write is initiated.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 35

NORMANDALE OPERATIONS



NOTES:  $\triangle$  READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 10 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE EXAMPLE CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

$\triangle$  ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUS WITH READ GATE.

FIGURE 13. TYPICAL TIMING WITH ADDRESS MARK

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 36

NORMANDALE OPERATIONS

## 6. AM Enable {Bit 5} {See Note}

The AM {Address Mark} Enable line, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks {see Figure 13}. When AM Enable is true while Write Gate is true, the writer will stop toggling and erase the data, creating an Address Mark. Write Fault detection in the unit is inhibited by this signal.

When AM Enable is true while Read Gate is true, an analog voltage comparator detects the absence of read signal. If the duration of the erased area is greater than 16 bits, an Address Mark found signal will be issued.

NOTE: If Address Mark is not used, Bit 5 must be held inactive during Control Select functions.

Address Mark should be 3.0 to 3.5 bytes in length with no transitions.

## 7. RTZ {Bit 6}

A 250 ns minimum, 1.0 ms maximum pulse, sent to the SMD will cause the actuator to seek track 0, reset the Head Register and clear the Seek Error flip-flop.

This seek is significantly longer than a normal seek to track track 0, and should only be used for recalibration, not Data acquisition.

## 8. Data Strobe Early {Bit 7}

When this line is true, the SMD PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

## 9. Data Strobe Late {Bit 8}

When this line is true, the SMD PLO Data Separator will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line is false.

NOTE: The Data Strobe and Carriage Offset signals are intended to be used as an aid to recover marginal data. The carriage and data strobe position return to nominal when the respective signals go false. A carriage offset will result in loss of 0n Cylinder and Seek End for a period of 3.2 ms maximum {see Figure 12}. The maximum time for the carriage to move from forward to reverse offset or vice versa does not exceed 7 ms. Data can not be written while in the offset mode.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 37

NORMANDALE OPERATIONS

## 10. Release {Bit 9} {Dual Channel Only}

Enabling this line will release channel reserve and Channel Priority Select Reserve in the SMD, making alternate channel access possible after selection by the other channel ceases. If the unit is desired to function with "Reserve Timer" feature, release will occur 500 ms {nominal} following the deselection of the SMD. If a longer or shorter time is desired, the timer may be customer altered by changing a resistor and capacitor to obtain delays from 500 ns to 10 seconds. Enabling Release will always clear Reserve and allow alternate channel access independent of the Reserve Timer feature. The Reserve Timer is enabled by means of a switch in the logic chassis. Inhibiting the Reserve Timer causes the SMD to stay Reserved until specifically released by the operating channel. A unit is Reserved immediately upon selection, but may be released any time after 500 ns following selection. By means of a switch in the logic chassis, it is also possible to absolutely reserve an SMD to one or the other channels.

### 6.2.1.4 Priority Select {Bit 9} {Dual Channel Only}

When this line is true during Unit Select Tag {see 6.2.2.8}, the unit will be unconditionally selected and absolutely reserved by the respective channel providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the Priority Select function has been performed the respective channel has exclusive access to the drive. The opposite channel can gain access only after a release function has been performed on the selected channel. For timing see Figure 15B.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 38

NORMANDALE OPERATIONS

## 6.2.2 Individual Lines

### 1. Sector Mark

The Sector Mark is derived from the servo track. Timing integrity is maintained throughout seek operations (see Figure 14). The number of sectors per revolution is switch selectable and is determined by counting dibits. The switches are located on a card within the logic chassis. Each switch represents a fixed number of dibits when closed.

Switch:	0	1	2	3	4	5	6	7	8	9	10	11
No. of dibits:	1	2	4	8	16	32	64	128	256	512	1024	2048

To calculate the proper switch positions for the number of sectors desired, use the following formula:

$$\frac{\text{Dibits/Revolution}}{\text{No. Sectors}} - 1 = \text{dibit count/sector}$$

Example for 8 sectors:  $\frac{13440}{8} - 1 = 1679$

Close switch 10 = 1024

9 = 512

7 = 128

3 = 8

2 = 4

1 = 2

0 = 1

One dibit for SM Counter Reset  $\frac{1}{1680}$  dibits/sector

Each dibit is equivalent to 12 data bits.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 39

NORMANDALE OPERATIONS

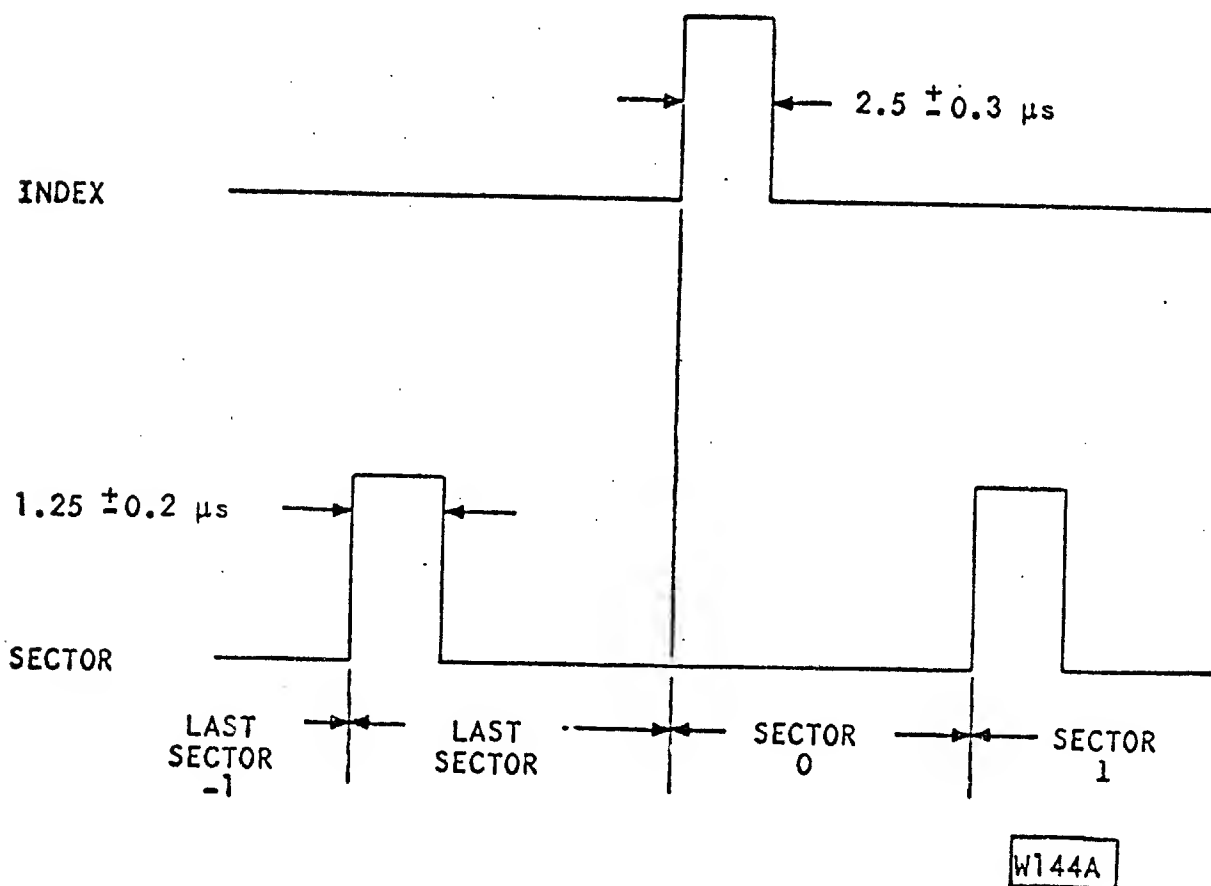


FIGURE 14. INDEX AND SECTOR TIMING

ENGINEERING  
SPECIFICATIONSPEC 64709300  
CD 4  
REV  
DATE  
PAGE 40

NORMANDALE OPERATIONS

## 2. Fault

When this line is true, a fault condition exists in the SMD. The following types of faults may be detected by the SMD: DC Power Fault, Head Select Fault, Write Fault, Write or Read while Off Cylinder, and Write Gate during a read operation. A fault condition will immediately inhibit the writer to prevent data destruction. The dc power fault indicates a below normal voltage from the positive or negative power supplies. The Head Select fault indicates that more than one head is selected. The Write fault indicates low for the absence of write current as well as the absence of write data.

This line may be cleared by Control Select, or Fault Clear on the Operator Panel, or Master Fault Clear on the Fault card {providing the fault no longer exists}. Faults are stored in individual flip-flops as a maintenance aid and may be cleared only by powering down dc power, or clearing the fault by means of the switch on the fault card.

## 3. Seek Error

When this line is true, a Seek Error has occurred. The error may only be cleared by performing an RTZ. This signal indicates that the unit was unable to complete a move within 500 ms, or that the carriage has moved to a position outside the recording field, or that an address greater than 823\* tracks has been selected. If an address greater than 823\* tracks is selected, the Seek Error signal will go true within 100 ns of the Cylinder Select tag, and the carriage movement is inhibited to not more than one track.

A Return-to Zero Seek command will clear the Seek Error condition, return the heads to cylinder zero, and enable an On Cylinder signal to the controller.

## 4. On Cylinder

This status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset will result in loss of On Cylinder for a period of 2.75 ms {nominal}. For a zero track seek, On Cylinder drops for 30  $\mu$ s {nominal}.

## 5. Index

This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typically 2.5  $\mu$ s {see Figure 14}. Timing integrity is retained throughout seek operations.

\*411 tracks for 9760/9764



# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 41

NORMANDALE OPERATIONS

## 6. Unit Ready

When true, and the unit is selected, this line indicates that the unit is up to speed, the heads are loaded, and no fault condition exists within the SMD. If, after a load sequence, dibits are not sensed within 350 ms, the heads will unload, and a fault will be indicated, and unit ready dropped. Further load attempts will require operator intervention to depress fault clear and cause heads to be reloaded.

## 7. Open Cable Detector

The open cable detect circuit (see Figure 8) disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

It is recommended that the controller circuitry have sufficient voltage margins and interlocks to prevent operation on the SMD before controller is Ready or prior to impending controller power failure. Relay logic and passive terminations sometimes aid this requirement. If 75110A transmitters are used to drive the Open Cable Detect line from the controller, two transmitters should be paralleled, and no 56 ohm termination resistance to ground should be used at the controller end.

## 8. Unit Select Tag

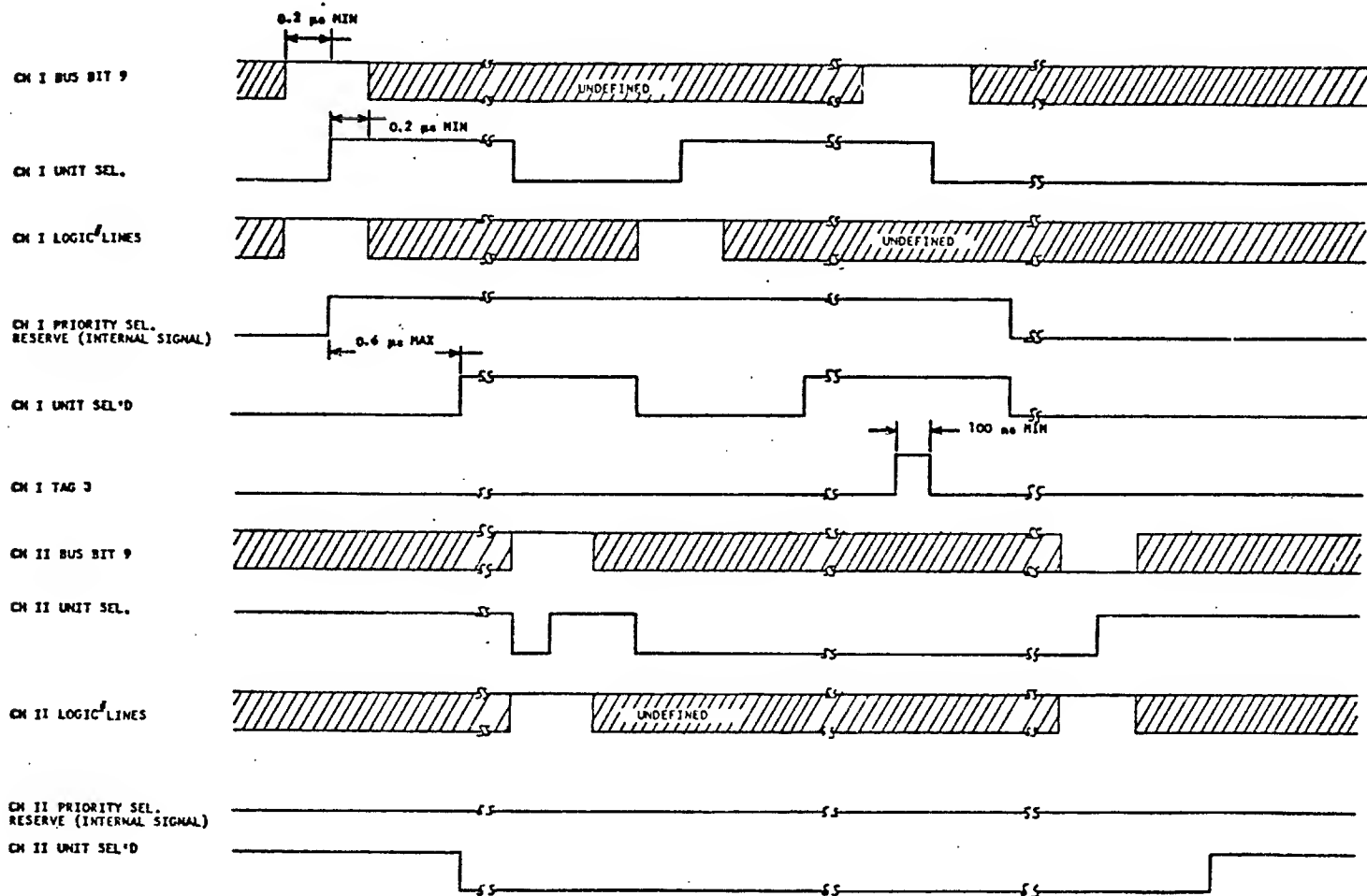
This signal gates the desired logic number into the logic number compare circuit. The unit will be selected internally 600 ns (maximum) after leading edge of this signal. For timing see Figure 15A and 15B. Note that this function must be edge triggered.

In Dual-Channel units, Unit Select tag also forces the SMD to be reserved to that channel, providing selection occurs. The reserve will not be cancelled unless by release command, Reserve Timer or dc power-down/power-up. If Bus Bit 9 and the desired logic number are present with Unit Select Tag, a Priority Select will be performed, see 6.2.1.4. The unit will be selected internally 600 ns (maximum) after leading edge of Unit Select Tag. For timing see Figure 15B.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 42

NORMANDALE OPERATIONS



## SEQUENCE OF EVENTS

1. CH II SELECTED
2. CH I PRIORITY SELECT
3. CH II PRIORITY SELECT
4. CH I RELEASE
5. CH II SELECT

1068

FIGURE 15A. SAMPLE PRIORITY SELECT TIMING

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 43

NORMANDALE OPERATIONS

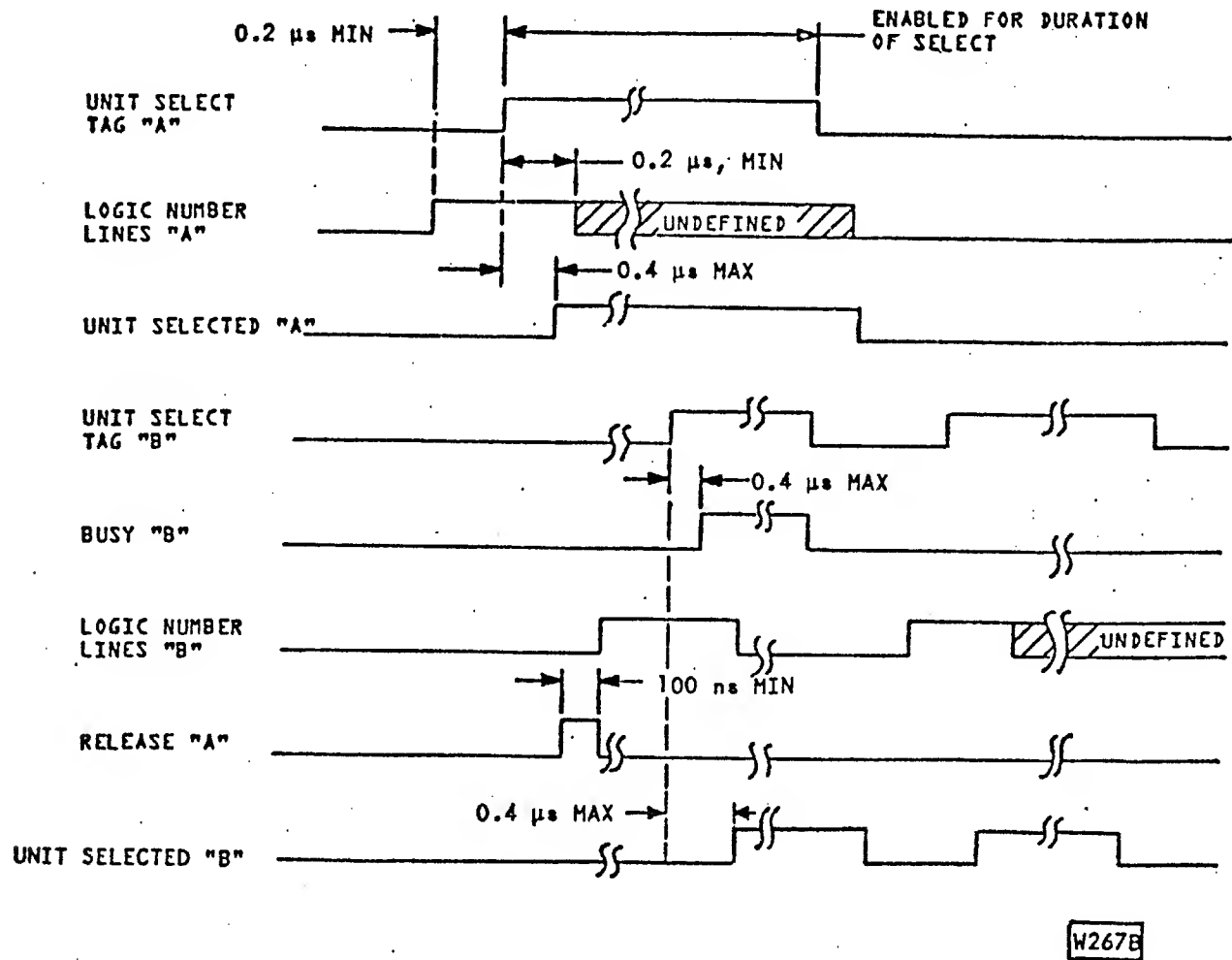


FIGURE 15B. LOGIC NUMBER SELECT AND TIMING DIAGRAM

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 44

NORMANDALE OPERATIONS

## 9. Unit Select {2<sup>0</sup>, 2<sup>1</sup>, 2<sup>2</sup>, and 2<sup>3</sup>}

These four lines are binary coded to select the logical number of one of fifteen SMDs. The unit number {0 through 14} is selectable by means of a logic plug on the Operator Panel in each individual unit. Care should be taken to have no duplicate logic plugs in the same system. A logic number of 15 is not allowed but may be used as maintenance select. Removing the logic plug from any unit results in a logic number 15.

## 10. Address Mark Found

Address Mark Found is a 9.0  $\mu$ s maximum pulse which is sent to the controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern.

The controller should drop the Address Mark Enable line {Bit 9} upon receiving Address Mark Found {AMF} and valid data will be presented on the I/O lines following the AMF pulse {see Figure 13}.

NOTE: Under certain conditions it is possible the SMD could issue a false Address Mark Found signal during an address mark search operation. This would occur if a media flaw existed which simulated the electrical characteristics of an address mark {at least 16 missing transitions followed by a zero}.

It is recommended provisions be made in system hardware or software to allow recovery from, or avoid the possibility of detecting false AMF signals.

## 11. Unit Selected

When the four Unit Select bit lines compare with the logic plug on the control panel, and when the leading edge of Unit Select tag is received, the Unit Selected line becomes true and is transmitted to the controller on the "B" cable {see Figure 15A/B}. Multiple Unit Selected responses on a daisy chain system indicate duplicate plugs have been installed.

## 12. Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a front panel LED, and sends a Write Protected signal to controller. Attempting to write while protected will cause a fault to be issued.

# ENGINEERING SPECIFICATION

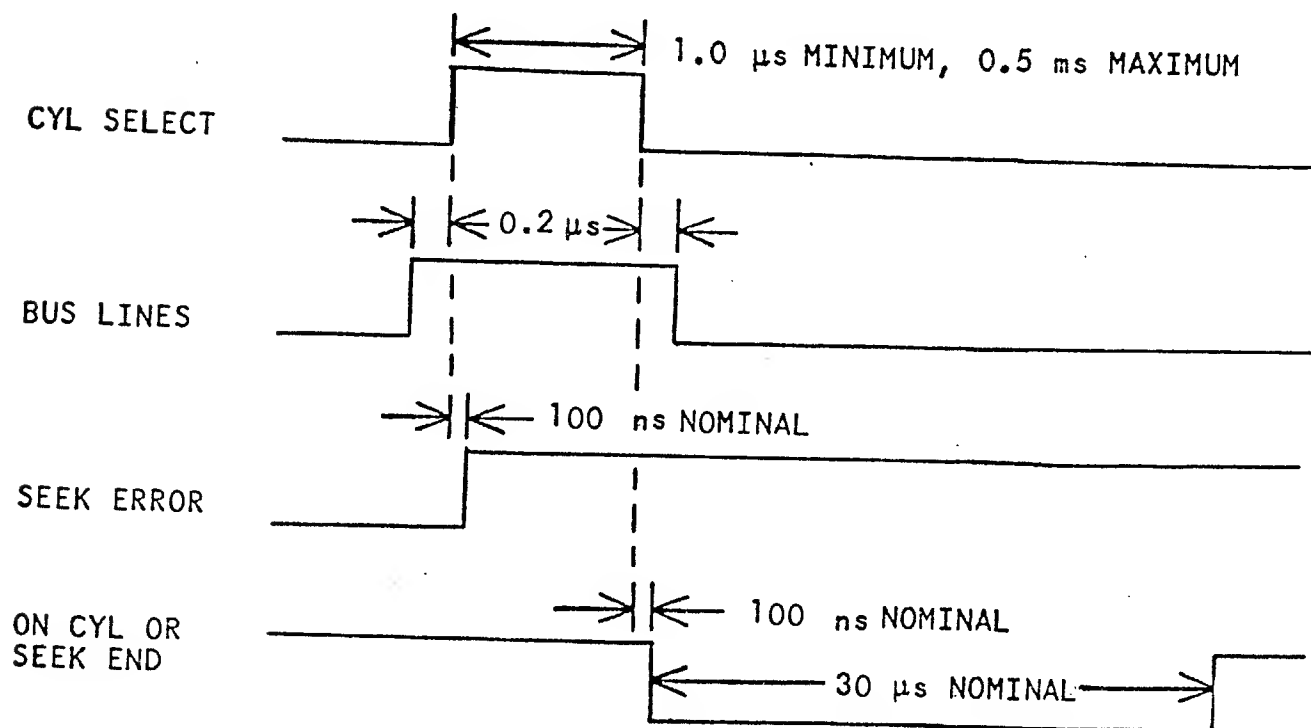
SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 45

NORMANDALE OPERATIONS

## 13. Seek End

Seek End is the combination of On Cylinder or Seek Error indicating that a seek operation has terminated. In Dual Channel Drives the Seek End signal sent to the unselected channel will normally be a constant one. However, if while the Drive is selected on a channel, and the opposite channel receives a select, this action will be noted by circuitry within the Drive. Then, when the selected channels Select and Reserve Latches are cleared, the Seek End signal sent to the waiting channel will go to a zero for 30  $\mu$ s. If an address greater than 823\* tracks has been selected, Seek End and On Cylinder will interrupt for 30  $\mu$ s nominal (see Figure 16).

\*411 for 9760/9764



W309A

FIGURE 16. SEEK END TIMING

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 46

NORMANDALE OPERATIONS

## 14. Power Sequencing {See Figures 17A/17B}

Power Sequencing requires ac and dc power on, START indicator on, and REMOTE START switch {switch selectable in SMD} in the Remote position. Applying ground to the Pick and Hold lines will cause the first SMD in sequence to power up. Once this SMD is up to speed, the Pick signal is transferred to the next active SMD and repeated until all active SMDs are powered up. Individual SMDs may be started and stopped once power sequencing is completed.

A power failure necessitates a new power up sequence.

When in Local Start mode, each SMD is independently operated by its respective START switch.

In the remote mode a Pick or Hold is considered to be present from the controller when a ground is present on "A" cable, Pin 29 for Pick and Pin 59 for Hold.

For 9760/9762 units this ground must sink 11 mA per unit. With 15 units on a system the current is 165 mA. The controller can provide this ground either through a mechanical contact {relay or switch} or through an electronic circuit.

For 9764/9766 units this ground must sink 60 mA per unit. With 8 units on a system the current is 480 mA.

## 15. Busy {Dual Channel Only}

If the SMD is already reserved and/or selected, a Busy signal will be issued to the "A" cable and unit selected will be issued on the "B" cable to the channel attempting the select. This Busy signal will be issued from the SMD at its I/O connector within 600 ns following the selection attempt, and remain at this status until Unit Select tag is dropped or the unit is no longer busy. Unit Selected should be used to enable Busy in the controller.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 47

NORMANDALE OPERATIONS

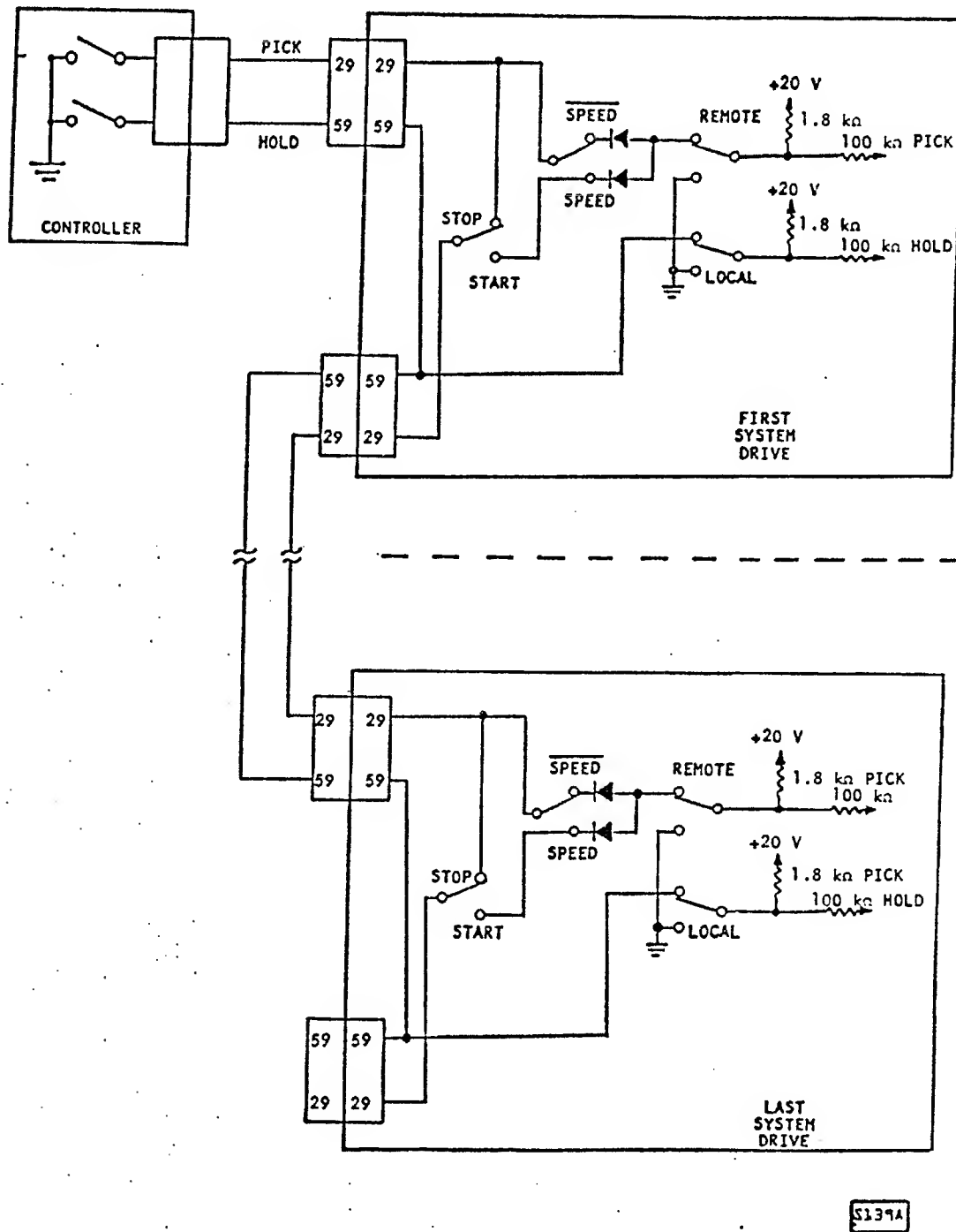


FIGURE 17A. 9760/9762 SEQUENCE POWER LINES

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 48

NORMANDEALE OPERATIONS

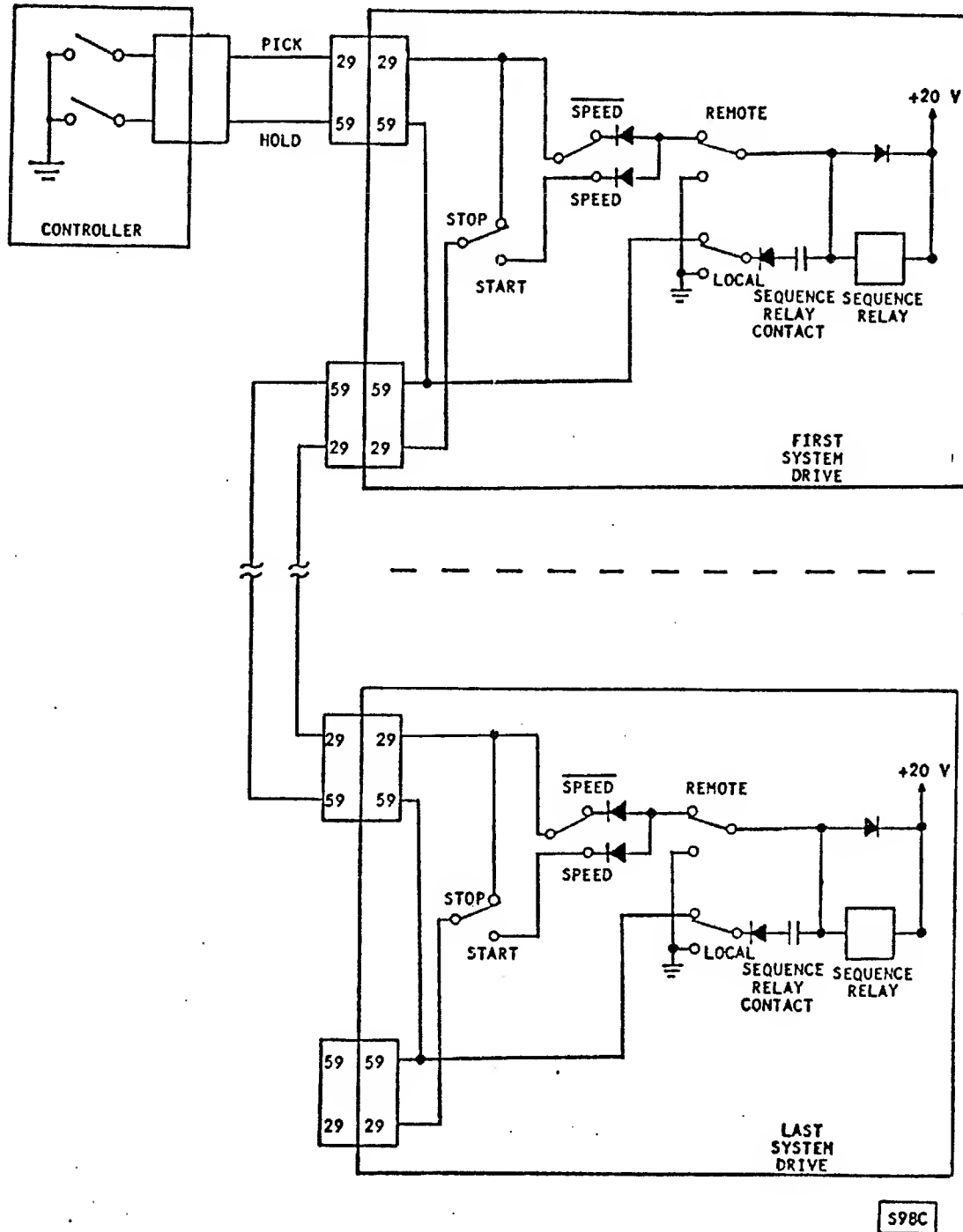


FIGURE 178. 9764/9766 SEQUENCE POWER LINES



# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 49

NORMANDALE OPERATIONS

## 6.2.3 Data and Clock Lines

### 1. Write Data

This line carries data which is to be recorded on the disk pack.

### 2. Servo Clock

The Servo Clock is a phase-locked 9.677 MHz clock generated from the servo track dibits {see Figure 18{A}}. Servo Clock is available at all times {not gated with Unit Select}.

### 3. Read Data

This line transmits the recovered data as NRZ form data {see Figure 18{B}}.

### 4. Read Clock

The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data as specified in Figure 18{B}. This signal is transmitted continuously, and is in phase sync within 9  $\mu$ s after Read Gate.

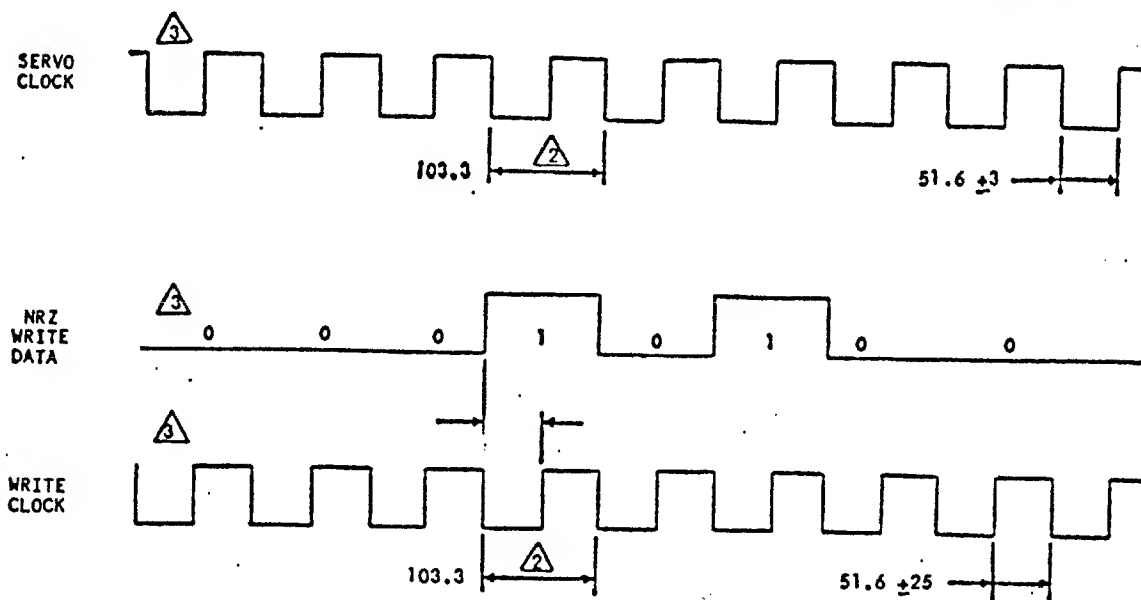
### 5. Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ data as illustrated in Figure 18{A}. The Write Clock is the Servo Clock retransmitted to the SMD by the controller, during a write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 ns prior to Write Enable.

# ENGINEERING SPECIFICATION

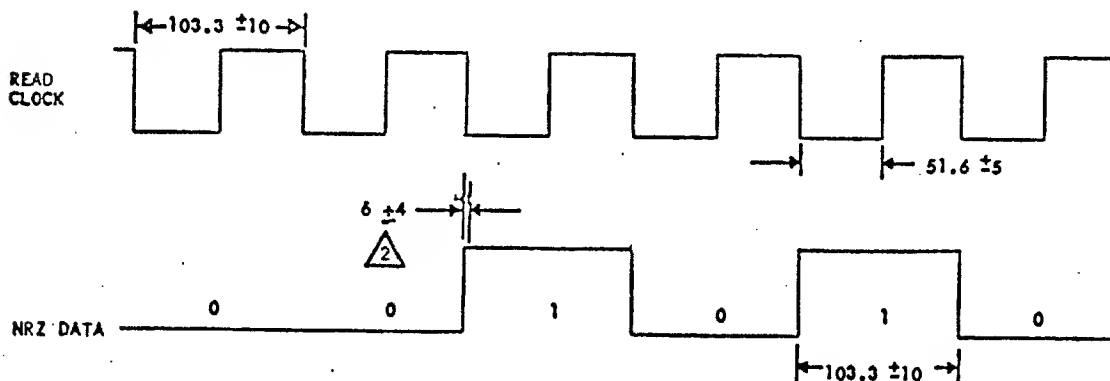
SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 50

NORMANDALE OPERATIONS



NOTES:

- 1 ALL TIMES IN ns.
- 2 SIMILAR PERIOD SYMMETRY IS  $\pm 2$  ns. AT I/O CONNECTOR IN DRIVE, SPEED VARIATION TOLERANCE IS  $\pm 5\%$  CONSISTING OF:
  - VARIATIONS BETWEEN INNER AND OUTER CYLINDER, INPUT POWER RANGES, MOTOR-TO-MOTOR VARIATIONS AND HUNTING. APPLIES WHEN ON CYLINDER.
  - DYNAMIC JITTER ON BYTE-TO-BYTE BASIS. APPLIES WHEN ON CYLINDER.
- 2 DIBIT SKEW AND DROP-OUT. APPLIES DURING SEEK. AT DRIVE I/O CONNECTOR.



NOTES: 1. ALL TIMES IN ns.

- 2 NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

## B. READ TIMING

W276D

FIGURE 1B. DATA TIMING

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 51

NORMANDALE OPERATIONS

## 6.3 Data Format and Data Control Timing

The Record Format on the disk is under control of the controller. The index and sector pulses are available for use by the controller to indicate the beginning of a track or sector. Suggested formats for fixed and variable sector data records are shown in Figures 19A/19B.

Some hardware-oriented constraints must be recognized when designing a format. The following is a list of those format parameters:

### 1. Beginning-of-Record Tolerance

This tolerance must be provided to allow for worst case conditions of head skew and circuit tolerances which may accrue during pack interchange.

This gap must be written with a minimum of 16 bytes of zeros.

### 2. Read PLO Synchronization

The synchronization time needed to allow the phase-locked oscillator to synchronize is 9  $\mu$ s of zeros.

### 3. Sync Pattern

The Sync Pattern consists of "one" bits indicating the beginning of the address or data area {one "one" bit is the minimum required}.

### 4. Write Driver Turn On

The Write Drive Turn On time is about 0.8  $\mu$ s or one byte. This time has to be accounted for in order to know where possible splice areas are located.

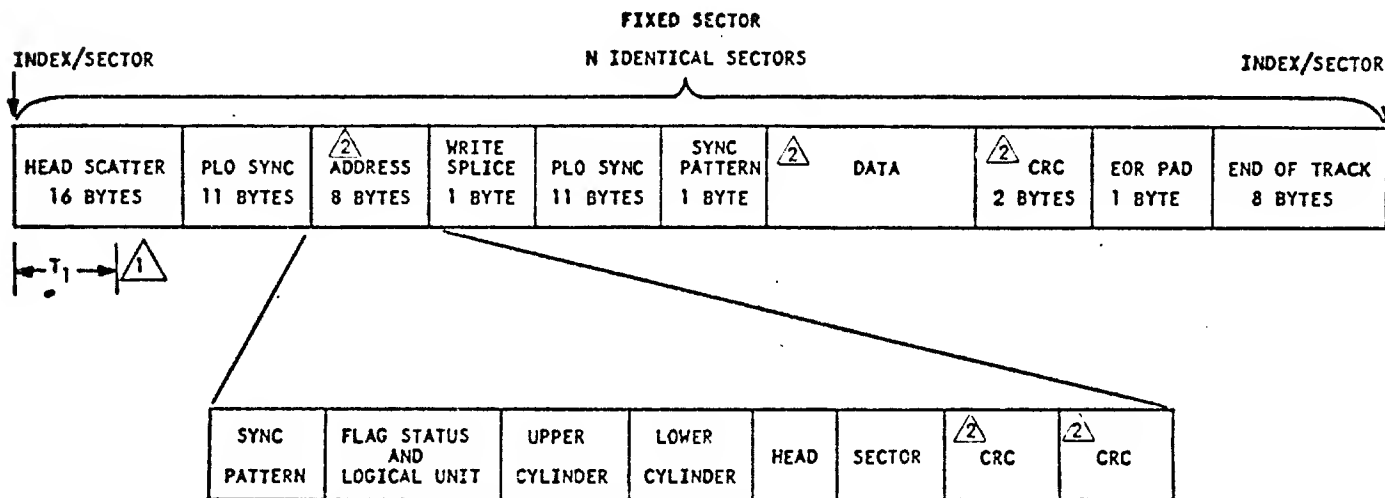
### 5. End-of-Record Tolerance

This tolerance is an eight byte pad of zeros which eliminates the possibility of destroying the end of a record written with a late displacement head. This is accomplished by writing an adjacent succeeding sector with an early head.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 52

NORMANDALE OPERATIONS



△<sup>1</sup> T<sub>1</sub> = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

△<sup>2</sup> THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

D47C

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20\,160}{64} - 59 = 256 \frac{\text{BYTES}}{\text{SECTOR}}$$

$$\text{DATA} = 256 \text{ BYTES/SECTOR}$$

$$\% \text{ EFFICIENCY} = \frac{256 \times 64}{20\,160} \times 100 = 81\%$$

FIGURE 19A. FIXED SECTOR FORMAT

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 53

INDEX

VARIABLE SECTOR WITH ADDRESS MARKS

N IDENTICAL SECTORS

INDEX

HEAD SCATTER 16 BYTES	ZEROES 1 BYTE	AM 3 BYTES	PLO SYNC 11 BYTES	ADDRESS <sup>2</sup> 8 BYTES	WRITE SPLICE 1 BYTE	PLO SYNC 11 BYTES	SYNC PATTERN 1 BYTE	DATA <sup>2</sup>	CRC <sup>2</sup> 2 BYTES	EOR PAD 1 BYTE	END OF TRACK 8 BYTES
--------------------------	------------------	---------------	----------------------	---------------------------------	------------------------	----------------------	------------------------	-------------------	-----------------------------	-------------------	-------------------------

T<sub>1</sub>

SYNC PATTERN	FLAG STATUS AND LOGICAL UNIT	UPPER CYLINDER	LOWER CYLINDER	HEAD	SECTOR	CRC <sup>2</sup>	CRC <sup>2</sup>
--------------	------------------------------	----------------	----------------	------	--------	------------------	------------------

2 THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

$$\% \text{ EFFICIENCY} = \frac{256 \times 68}{20 \times 160} \times 100 = 86\%$$

AA1836 1/77

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 54

NORMANDALE OPERATIONS

## 6.3.1 Write Format Procedure

Provisions must be made within the controller to format the disk.  
The following procedure is recommended for fixed sector formats:

### Procedure

1. Select desired unit, cylinder, head, and sector.
2. The controller must provide a 5  $\mu$ s minimum delay between selecting a head and initiating a search for leading edge of sector. This delay will ensure that the unit will be ready to write when the sector leading edge is detected.
3. Search for leading edge of desired sector.
4. Detect leading edge of selected sector.
5. Immediately bring up Write Gate and start writing zeros.
6. Write all zeros for head scatter and PL0 sync areas {27 bytes}.
7. Write a sync pattern, the address, and the address checkword.
8. Write all zeros for Write Splice gap and PL0 Sync field {12 bytes}.
9. Write a sync pattern, the Data Field, the two byte data field checkword, and the one byte pad at the end of the checkword. The Data Field should be written with all ones or preferably a worst case pattern.
10. The end tolerance gap is the only part of the format where there may be erased areas with no write data. If erased areas occur in Gap 2 there may be problems in recovering the data following this gap.
11. If the next sector of the same track is to be formatted and the head is not deselected, the Write Gate should be left on. In this case, the controller should write all zeros in the tolerance gap. If Write Gate is dropped, it should not be raised again within 2  $\mu$ s.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 55

NORMANDALE OPERATIONS

## 6.3.2. Control Timing {See Figure 20}

### 1. Read

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate forces the phase-locked oscillator to synchronize on an all zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled  $60 \pm 4$  clock counts after the leading edge of Index or Sector.

The sync pattern search may begin 88 Servo Clock counts after the leading edge of Read Gate.

Head switching and read amplifier stabilization {see Figure 20{A}} shows the latest acceptable time at which a head can be selected in order to read the next successive sector {with the format described in 6.3}.

Data I/O lines may not have valid data until 9  $\mu$ s from leading edge of Read Gate, due to phase lock synchronizing time.

Ensure that there will be no splice area after Read Gate is brought up even under worst case pack interchange conditions.

### 2. Write Data Field

The control line associated with a write operation is Write Gate.

The sector address must always be read and verified prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the PL0 sync field and sync pattern.

The controller must provide a three bit internal delay {approximately 0.3  $\mu$ s} between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal {see Figure 20{B}}. This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

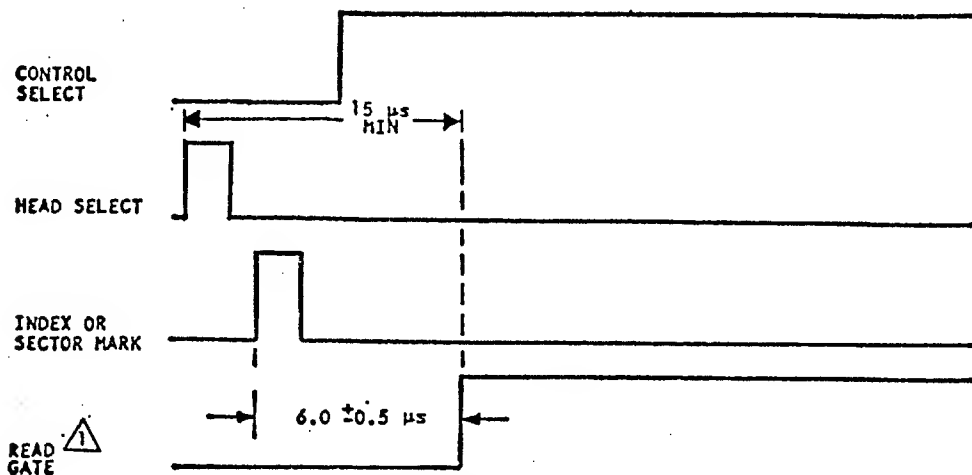
Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, Write Gate is raised immediately upon sensing Index or Sector. During a record update, Write Gate is raised within two bits of the last bit of an address.

# ENGINEERING SPECIFICATION

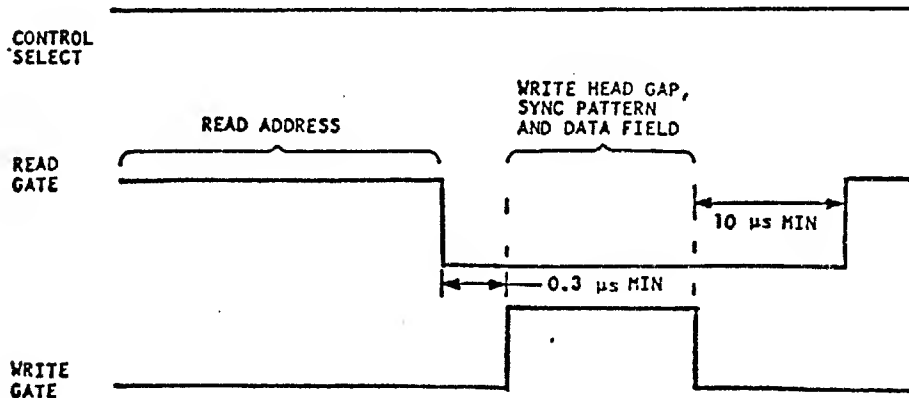
SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 56

NORMANDALE OPERATIONS



IF A READ OPERATION IS TO BE PERFORMED AFTER INDEX OR SECTOR, READ GATE MUST NOT OCCUR LATER THAN  $6.0 \pm 0.5 \mu s$  AFTER THE LEADING EDGE OF INDEX OR SECTOR.

## A. TYPICAL READ CONTROL TIMING



## B. TYPICAL WRITE CONTROL TIMING

W359A

FIGURE 20. CONTROL TIMING



# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 57

NORMANDALE OPERATIONS

## 7.0 CONTROLS AND INDICATORS

### 7.1 Operator Panel

<u>NAME</u>	<u>TYPE</u> <u>LIGHT</u> <u>SW</u>	<u>FUNCTION</u>
START	X X	Indicates conditions of START switch and top cover interlocks. The switch starts or stops the unit.
READY	X	Indicates Unit Ready status, i.e., pack is up to speed, the heads are loaded, and no fault condition exists within the unit.
FAULT	X X	Indicates any fault condition. The switch clears the fault flip-flop.
WRITE PROTECT	X X	Inhibits Writer.

### 7.2 Maintenance Switch and Indicators

<u>NAME</u>	<u>TYPE</u> <u>LIGHT</u> <u>SW</u>	<u>FUNCTION</u>
WRITE	X	Indicates that a write fault had occurred.
HEAD SELECT	X	Indicates that a multiple head select had occurred.
WRITE AND READ	X	Indicates write and read conditions existed simultaneously.
WRITE OR READ AND OFF CYL	X	Indicates write or read conditions existed during a seek operation {off cylinder}.
VOLTAGE	X	Indicates a below normal voltage existed.
FAULT CLEAR	X	Master clears all faults providing the fault no longer exists.

The indicators listed above are located on the fault card in the logic chassis and are visible only when the SMD top cover is in the maintenance position. The indicators are cleared by the switch on the fault card or by removing dc power.

# ENGINEERING SPECIFICATION

SPEC 64708300  
CD 4  
REV  
DATE  
PAGE 58

NORMANDALE OPERATIONS

## 7.3 Channel Select and Reserve Switches and Indicators

<u>NAME</u>	<u>TYPE</u>		<u>FUNCTION</u>
	<u>LIGHT</u>	<u>SW</u>	
DI/NRM		X	Switch will disable Channel I or allow Channel I to be selected.
DII/NRM		X	Switch will disable Channel II or allow Channel II to be selected.
ABR/RTM		X	In ABR position once drive is selected it must be released in order for reserve to drop. In RTM position once drive is deselected, reserve will drop after 500 ms.
Ch. I Sel		X	Indicates Channel I is selected.
Ch. I Res		X	Indicates Channel I is reserved.
Ch. II Sel		X	Indicates Channel II is selected.
Ch. II Res		X	Indicates Channel II is reserved.

## 7.4 Elapsed Time Meter

A running time meter is provided and is active when the ac power is applied to the unit and the main circuit breaker is closed.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 59

NORMANDALE OPERATIONS

## 8.0 PHYSICAL SPECIFICATIONS

The nominal dimensions and weights of Table 3 do not include the shipping container or packaging.

TABLE 3. PHYSICAL SPECIFICATIONS

DESCRIPTION	PEDESTAL CABINET 9760/9762	SMD RACK MOUNT 9760/9762	SMD DRAWER MOUNT 9760/9762	SMD ACOUSTIC CABINET 9760/9762	SMD ACOUSTIC CABINET 9764/9766	DESK MOUNT 9760/9762
HEIGHT	34.0 IN.	10.5 IN.	11.0 IN.	36.2 IN.	36.2 IN.	10.5 IN.
DEPTH	34.0 IN.	30.0 IN.	30.6 IN.	36.0 IN.	36.0 IN.	30.0 IN.
WIDTH	19.0 IN.	19.0 IN.	19.3 IN.	22.0 IN.	23.0 IN.	17.3 IN.
WEIGHT	243 LB	160 LB	227 LB *	340 LB	556 LB	165 LB
FLOOR LOAD AT EACH REST PAD	61.0 LB	40 LB		85 LB	138 LB	41.3 LB

\*Weight includes items described in drawer mount {see 3.2.1.3}.

T19A

## 9.0 RELIABILITY AND SERVICE GOALS

### 9.1 Mean Time Between Failure

Following an initial period of 200 hours, the Mean Time Between Failure exceeds 3000 hours for units manufactured in the first year of production and 3500 hours for units manufactured in the second year. For units manufactured after the second year, the MTBF exceeds 4000 hours. The following expression defines MTBF:

$$MTBF = \frac{\text{Operating Hours}}{\text{No. of Equipment Failures}}$$

Operating hours means total time meter hours less any maintenance time. Equipment failure means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by the equipment. To establish a meaningful MTBF, operation hours must be greater than 5200 and shall include field performance data from all field sites.

For the purpose of this specification, equipment failures are defined as those failures necessitating repairs, adjustments or replacements on an unscheduled basis. Essentially, the term equipment failure implies that emergency maintenance is required because of hardware failure or substandard performance.

# ENGINEERING SPECIFICATION

SPEC 54709300  
CD 4  
REV  
DATE  
PAGE 60

NORMANDALE OPERATIONS

## 9.2 Mean Time to Repair

The mean time to repair does not exceed 1.5 hours; it is defined as the time for an adequately trained and competent serviceman to diagnose and correct a malfunction.

## 9.3 Preventive Maintenance Time

Routine scheduled preventive maintenance does not exceed one-half hour per 1000 hours of operating time per spindle. This maintenance shall be performed by suitably trained and competent customer personnel. The schedule for preventive maintenance is based on procedures recommended by Control Data Corporation.

## 9.4 Service Life

The Storage Module Drive is designed and constructed to provide a useful life of five years before factory overhaul or replacement is required. Repair or replacement of major parts is permitted during the lifetime.

## 10.0 INSTALLATION AND MAINTENANCE

Required connections to the device are power {dependent upon options selected}, signal cables and a system ground consistent with CDC STD 1.30.023. The physical requirements are adequate clearances for maintenance and air intake/exhaust. Detailed instructions are found in the equipment maintenance manuals.

### 10.1 Power Requirements

#### 10.1.1. Primary Power Requirements

The primary voltage and current requirements are shown in Tables 4 and 5. Start up current is shown in Figure 21{A}/{B}.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 61

NORMANDALE OPERATIONS

TABLE 4. PRIMARY VOLTAGE REQUIREMENTS

UNIT TYPE	VOLTAGE {V ac}	TOLERANCE {V ac}	FREQUENCY {Hz}	TOLERANCE {Hz}
9760/9762	100	±10	60	+0.6, -1.2
9760/9762	120	+8.0, -18	60	+0.6, -1.0
9764/9766	200	±20	60	+0.6, -1.2
9764/9766	208	+14.6, -29	60	+0.6, -1.0
9764/9766	230*	+16.0, -32	60	+0.6, -1.0
9760/9762	100	±10	50	+0.5, -1.0
9764/9766	200	±20	50	+0.5, -1.0
All	220	+15.0, -25	50	+0.5, -1.0
All	240*	+17.0, -27	50	+0.5, -1.0

\*Internal jumper must be changed.

TABLE 5. PRIMARY CURRENT REQUIREMENTS

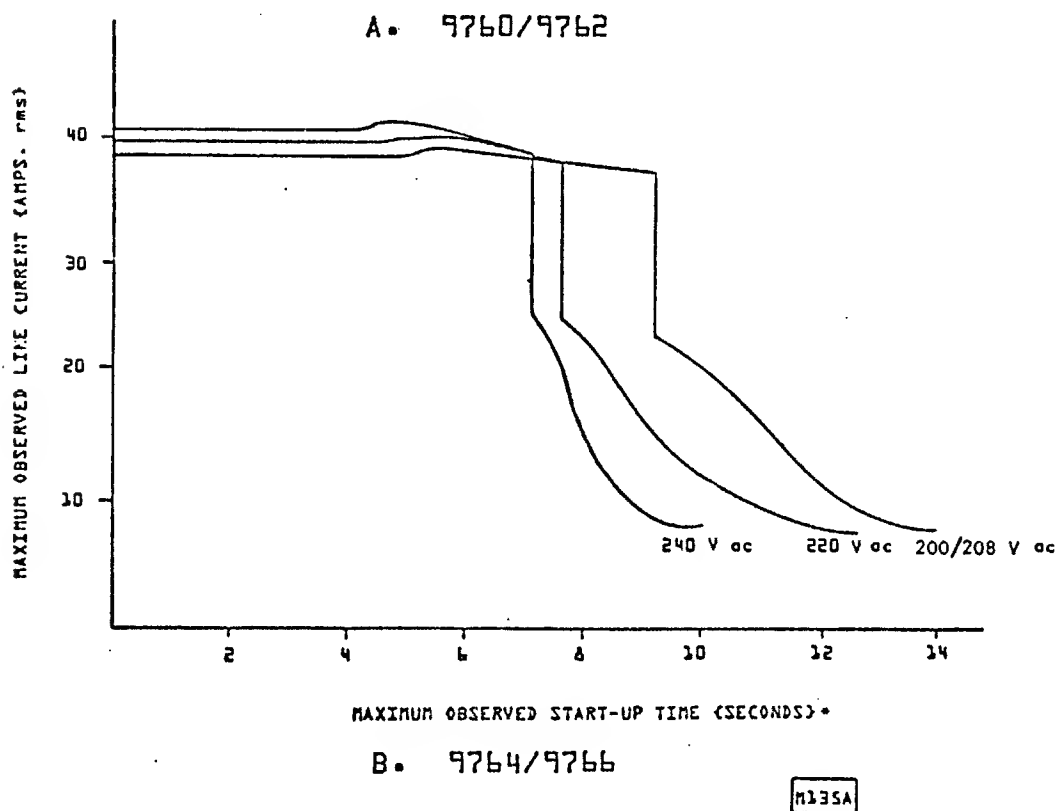
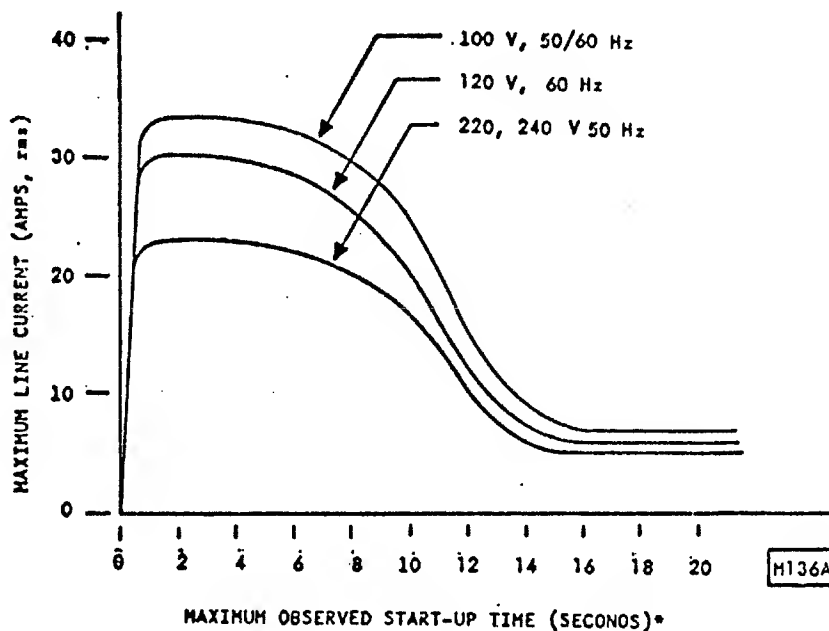
UNIT STATUS	LINE CURRENT*	CONSUMPTION*		AC POWER
		kW	BTU/hr	{V ac-Hz}
Disks and carriage in motion	10.03 amps {9760/9762}	0.875	2986	100-60
	10.10 amps {9760/9762}	0.877	2993	100-50
	8.90 amps {9760/9762}	0.876	2989	120-60
	8.60 amps {9764/9766}	1.40	4778	200-50/60
	4.60 amps {9760/9762}	0.838	2860	220-50
	4.10 amps {9760/9762}	0.837	2856	240-50
	8.65 amps {9764/9766}	1.46	4983	208-60
	7.80 amps {9764/9766}	1.45	4949	230-60
	9.18 amps {9764/9766}	1.50	5119	220-50
Disks not in motion {standby}	8.56 amps {9764/9766}	1.51	5153	240-50
	3.06 amps {9760/9762}	0.276	942	100-60
	3.08 amps {9760/9762}	0.278	949	100-50
	2.60 amps {9760/9762}	0.274	935	120-60
	1.77 amps {9764/9766}	0.367	1253	200-50/60
	1.30 amps {9760/9762}	0.281	959	220-50
	1.19 amps {9760/9762}	0.283	966	240-50
	1.77 amps {9764/9766}	0.367	1253	208-60
	1.63 amps {9764/9766}	0.370	1263	230-60
	1.80 amps {9764/9766}	0.348	1188	220-50
	1.79 amps {9764/9766}	0.349	1191	240-50

\*The numbers given in this table are maximum values.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 62

NORMANDALE OPERATIONS



\*These graphs indicate typical maximum values, and are not to be considered as absolute maximums.

FIGURE 21. LINE CURRENT VERSUS START-UP TIME

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 63

NORMANDEALE OPERATIONS

## 10.1.2 Power Cable and Connector for 9760/9762

The customer may elect to hardwire or use his own connector consistent with his system's ac distribution. The power cable is 6 ft long. Pin Configuration is shown in Figure 22.

<u>DESCRIPTION</u>	<u>CDC P/N</u>	<u>NEMA CONFIGURATION</u>
120 V, 15A, 60 Hz, 1Ø 2 pole, 3 wire, male connector	24531601	5-15 P

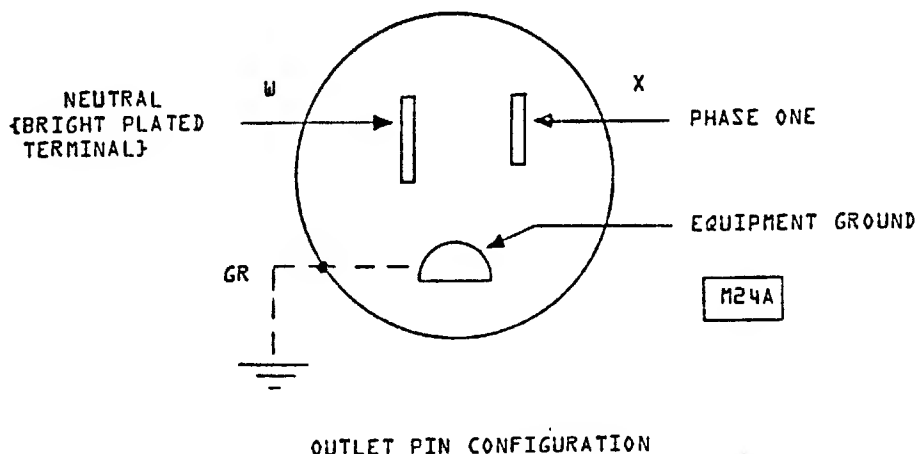


FIGURE 22. INPUT POWER CONNECTOR {120 V ac, 60 Hz}

A color-coded power cable is supplied with the 50 Hz SMD, but the 50 Hz connector must be furnished by the user. The cable color code and unit power requirements are as follows:

<u>DESCRIPTION</u>	<u>COLOR-CODE</u>
220/240 V, 50 Hz	Brown - Phase One Blue - Neutral Green and yellow - AC Equipment Ground

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 64

NORMANDALE OPERATIONS

## 10.1.3 Power Cable and Connectors for 9764/9766

The SMD power cable is 12 ft long. Connectors are defined as:

DESCRIPTION	CDC P/N	HUBBEL P/N	NEMA CONFIGURATION
208/230 V, 20 A, 60 Hz 1Ø, 2 pole, 3 wire, locking male connector	94368003	2321	LB-20 P

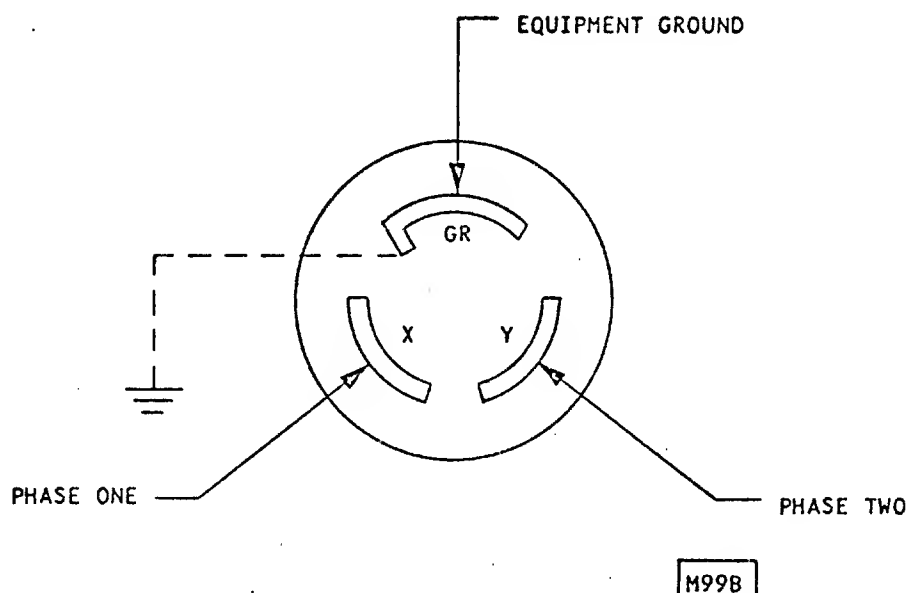


FIGURE 23. INPUT POWER CONNECTOR (208/230 V ac, 60 Hz)

The part numbers for mating connectors (connector body and outlet) are given below, but are not supplied with the drive and must be purchased separately.

	CONNECTOR BODY	OUTLET
CDC P/N	94368004	94368005
Hubble P/N	2323	2326
NEMA Configuration	LB-20 R	LB-20 R

A color-coded power cable is supplied with the 50 Hz SMD, but the 50 Hz connector must be furnished by the user. The cable color code and unit power requirements are as follows:

DESCRIPTION	COLOR-CODE
220/240 V, 50 Hz	Brown - Phase One Blue - Neutral or Phase Two Green and yellow - AC Equipment Ground



# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 65

NORMANDALE OPERATIONS

## 10.2 Grounding

The necessary installation requirements are power and signal cable connections to the SMD. A ground strap must be connected between the power supply dc grounds of the controller and SMDs. Detailed instructions are in the Equipment Maintenance Manual.

## 10.3 Environmental Limits

### 10.3.1 Temperature

#### a. Operating

59°F {15°C} to 104°F {40°C} with a maximum gradient of 12°F {6.7°C} per hour.

#### b. Transit {as packed for shipment}

Minus 40°F {-40°C} to 158°F {70°C} with a maximum gradient of 36°F {20°C} per hour.

### 10.3.2 Relative Humidity

#### a. Operating

20% to 80% R.H. {providing there is no condensation}.

#### b. Transit {as packed for shipment}

5% to 95% {providing there is no condensation}.

### 10.3.3 Altitude {actual or effective}

#### a. Operating

1000 ft {305 m} below sea level to 6500 ft {2000 m} above sea level.

#### b. Transit {as packed for shipment}

1000 ft {305 m} below sea level to 15 000 ft {4572 m} above sea level.

# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 66

NORMANDALE OPERATIONS

## 10.3.4 Vibration and Shock

### a. Operating

Equipment, as normally installed and positioned, meets the full specified performance while subject to the following conditions injected from the floor in a vertical direction:

1. Continuous vibration as indicated in Figure 24, operating curve A.
2. Intermittent shocks {2 per second or fewer} of up to 2 g not exceeding 10 ms in duration.

### b. Transit {as packed for shipment}

Equipment in an upright position will withstand the conditions of vibration and shock, base input only, as follows:

1. Vibration, as shown in Figure 24, nonoperating curve C.
2. Shocks of up to 20 g not exceeding 10 ms in duration. The time between consecutive shocks cannot be less than 5 seconds.

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 67

NORMANDALE OPERATIONS

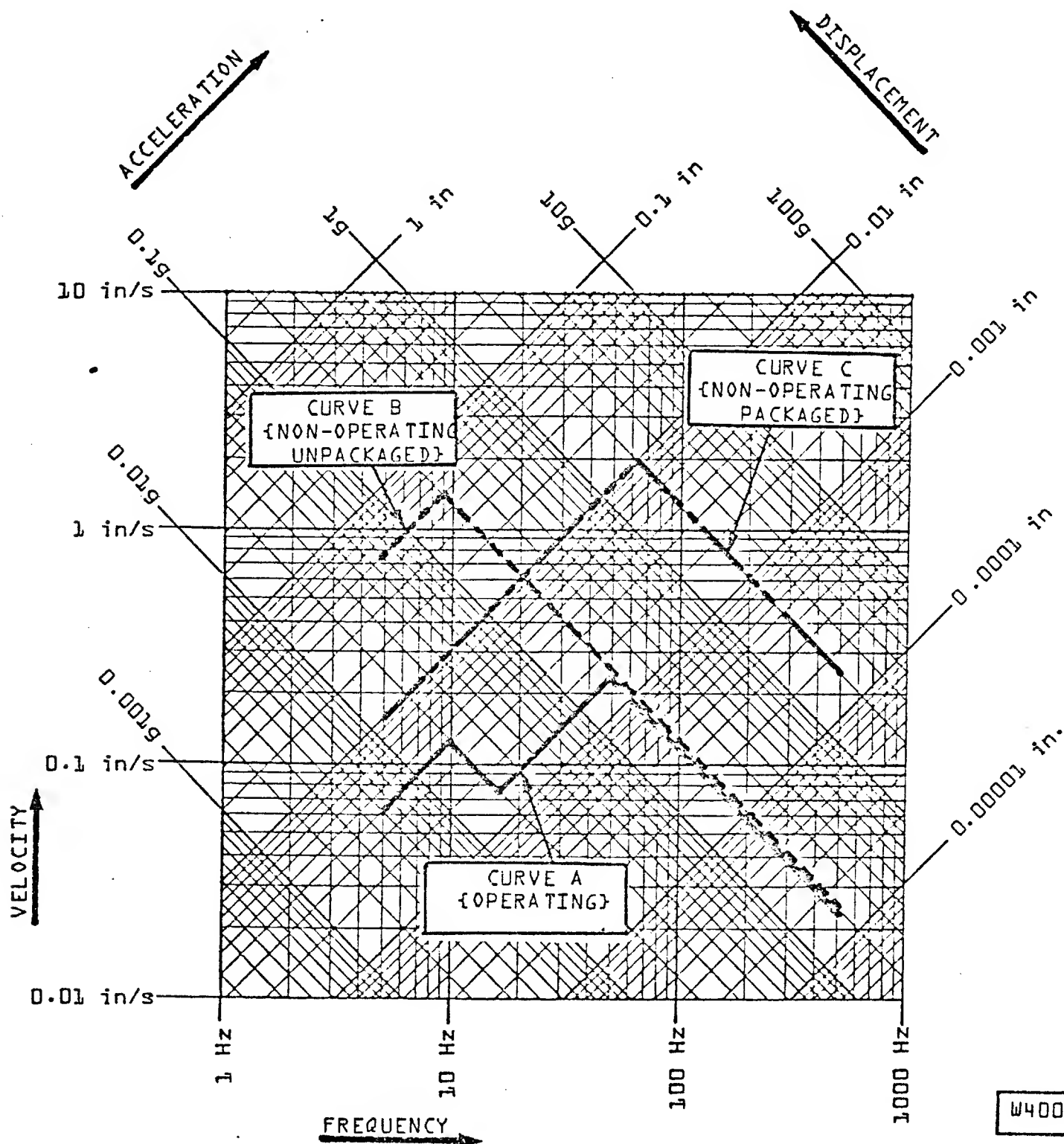
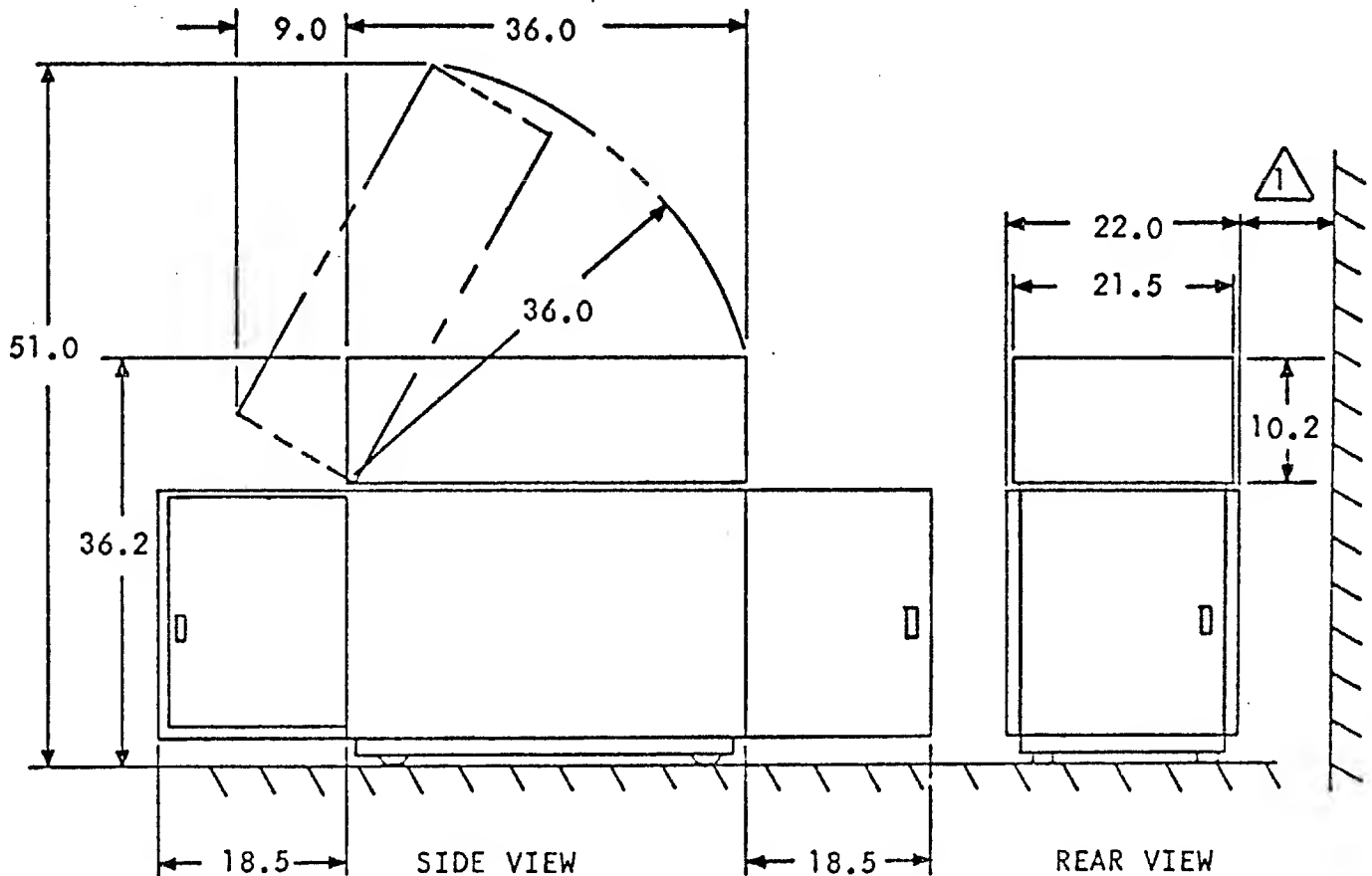


FIGURE 24. VIBRATION LEVELS

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 68

NORMANDALE OPERATIONS



F85A



IF NEXT OBSTACLE (WALL OR OTHER EQUIPMENT) IS GREATER THAN 36 INCHES HIGH, A MINIMUM SERVICE AREA OF 19 INCHES IS REQUIRED FOR MAINTENANCE, MEASURED FROM REAR TO THE RIGHT SIDE OF THE SMD.



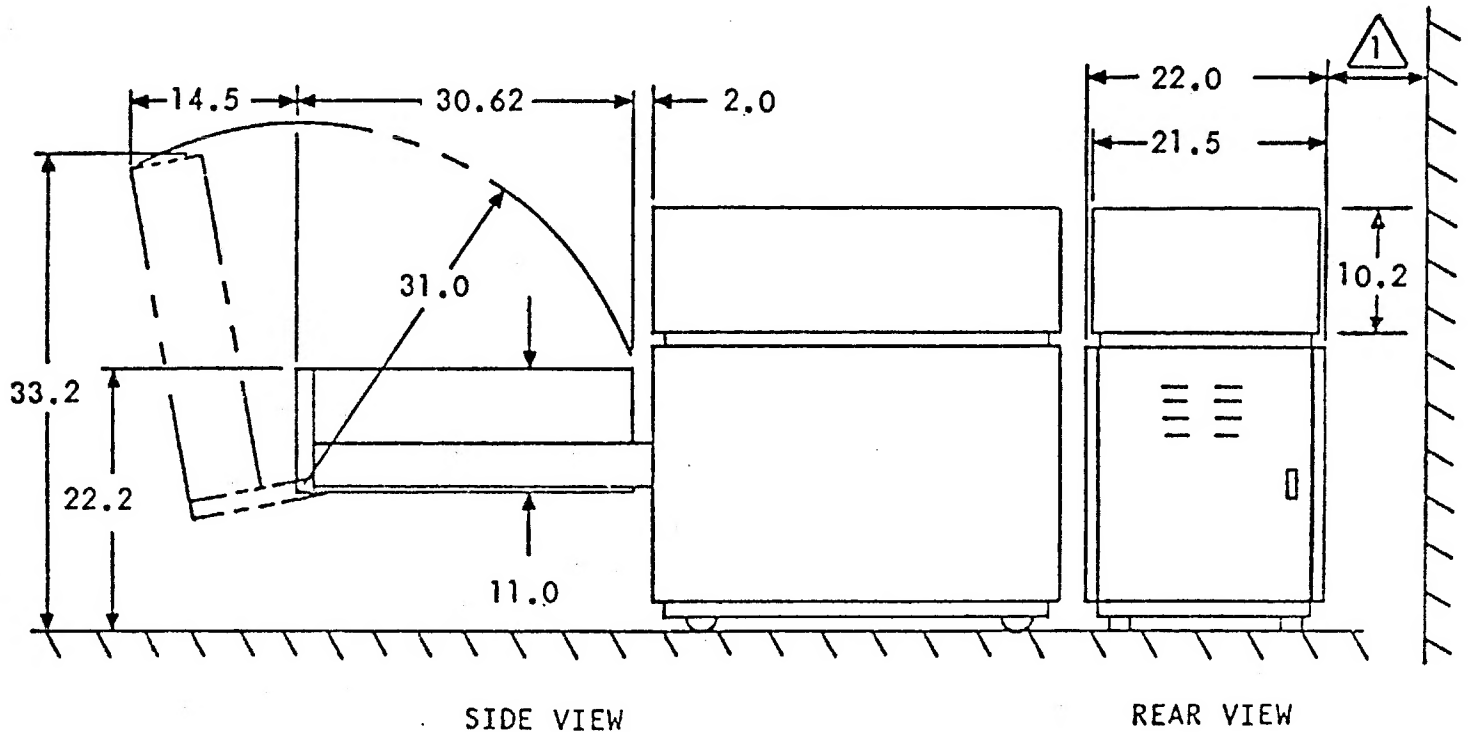
DIMENSIONS ARE NOMINAL AND INTENDED FOR SITE PLANNING USE ONLY.

FIGURE 25A. 9760/9762 ACOUSTIC CABINET DETAIL

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 69

NORMANDALE OPERATIONS



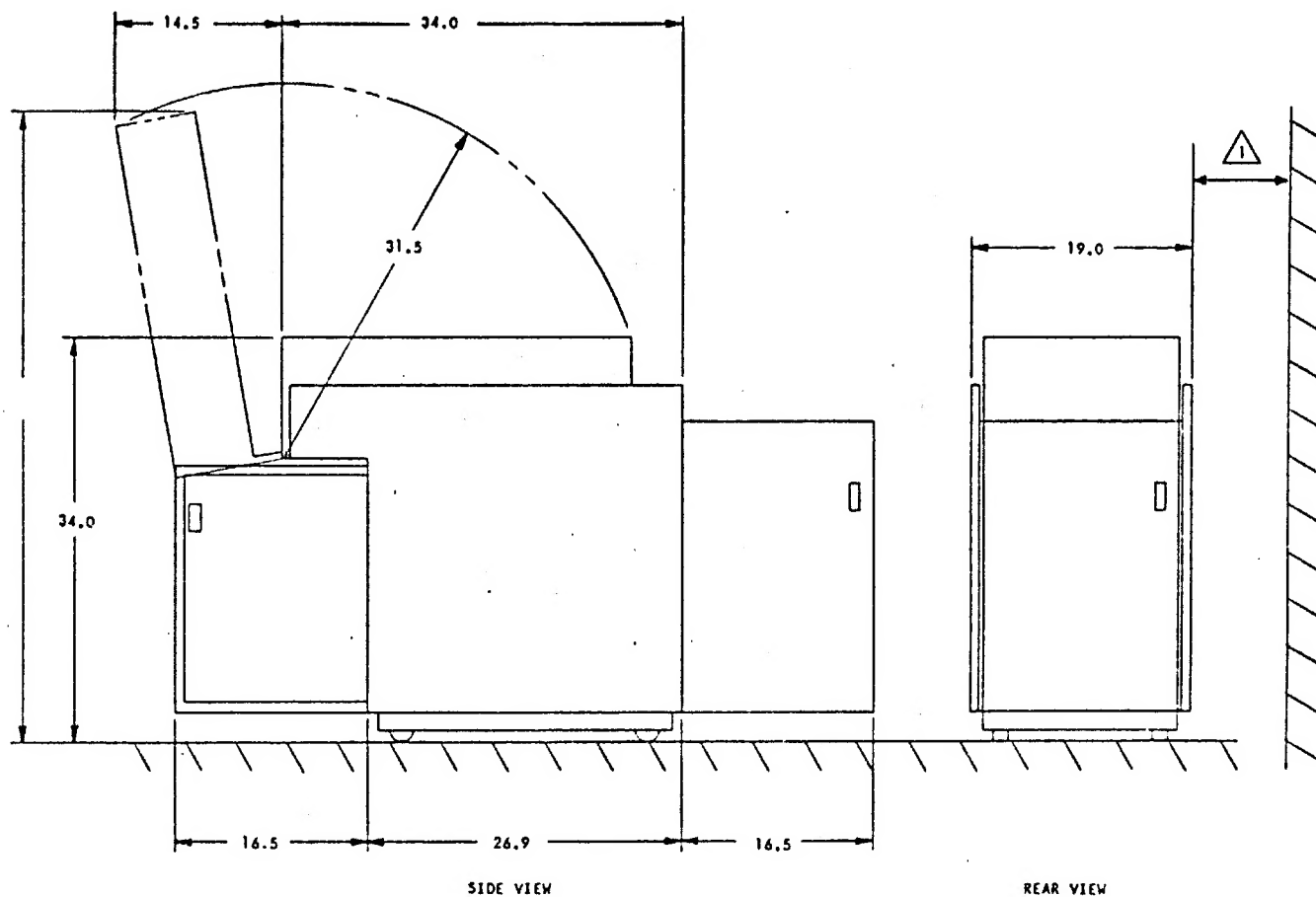
F47E

FIGURE 25B. 9760/9762 ACOUSTIC CABINET DETAIL,  
DRAWER MOUNT SMD

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 70

NORMANDALE OPERATIONS



- 1 IF NEXT OBSTACLE (WALL OR OTHER EQUIPMENT) IS GREATER THAN 36 INCHES HIGH;  
 THEN A MINIMUM SERVICE AREA OF 19 INCHES IS REQUIRED FOR MAINTENANCE,  
 MEASURED FROM THE REAR TO THE RIGHT SIDE OF THE SMO.
- 2 DIMENSIONS ARE NOMINAL AND INTENDED FOR SITE PLANNING USE ONLY.

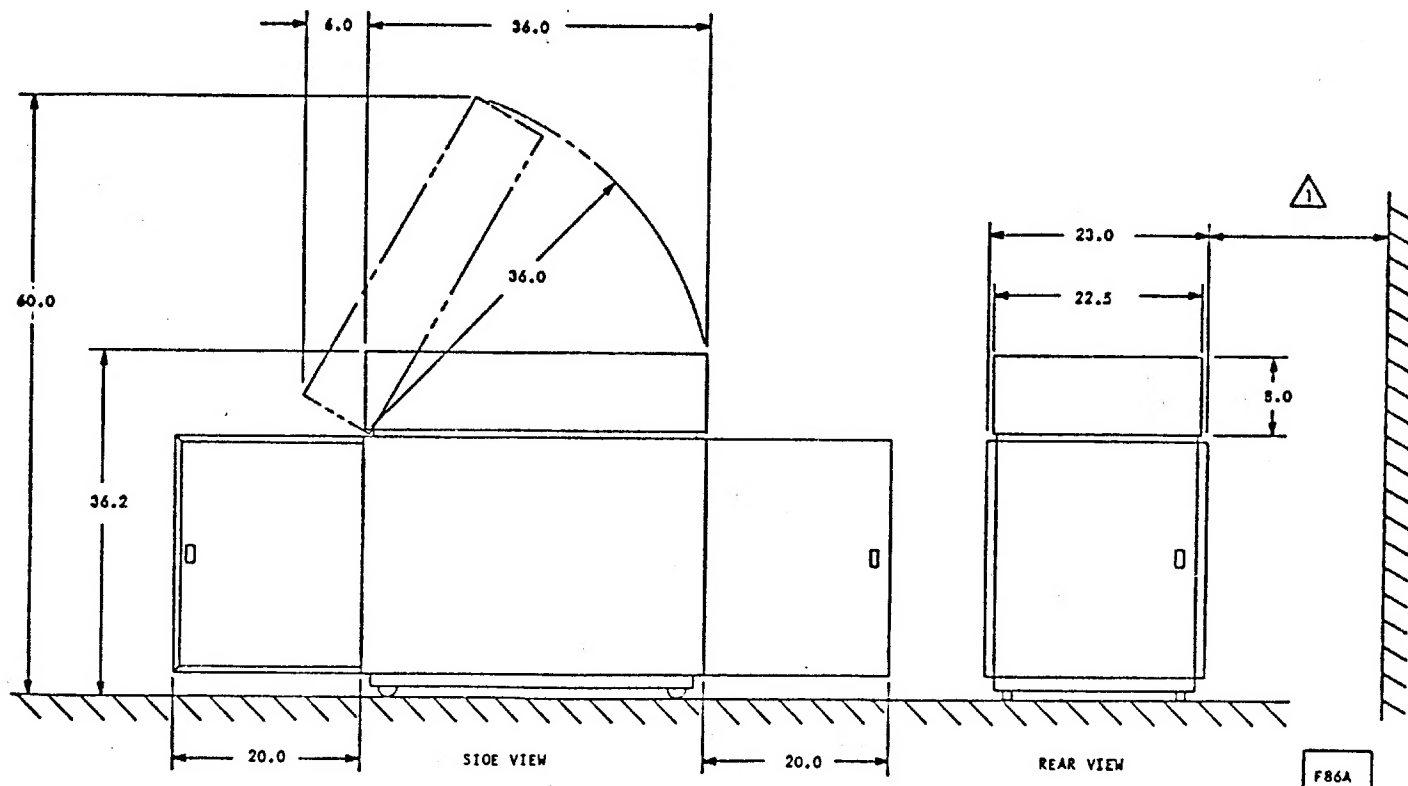
F478

FIGURE 26. 9760/9762 PEDESTAL CABINET MOUNT DETAIL

# ENGINEERING SPECIFICATION

SPEC 64709300  
 CD 4  
 REV  
 DATE  
 PAGE 71

NORMANDALE OPERATIONS



1 IF NEXT OBSTACLE (WALL OR OTHER EQUIPMENT) IS GREATER THAN 36 INCHES HIGH, A MINIMUM SERVICE AREA OF 19 INCHES IS REQUIRED FOR MAINTENANCE, MEASURED FROM REAR TO THE RIGHT SIDE OF THE SMO.

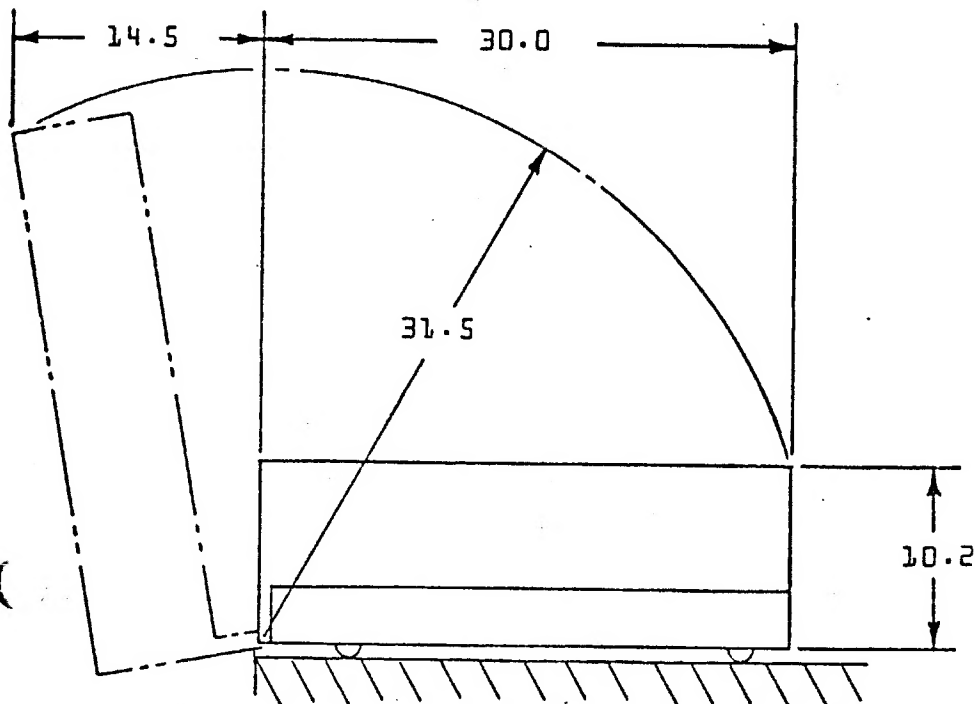
2 DIMENSIONS ARE NOMINAL AND INTENDED FOR SITE PLANNING USE ONLY.

FIGURE 27. 9764/9766 ACOUSTIC CABINET DETAIL

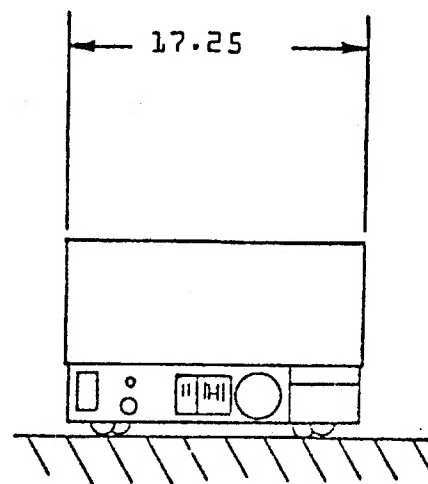
# ENGINEERING SPECIFICATION

SPEC 64709300  
CD 4  
REV  
DATE  
PAGE 72

NORMANDALE OPERATIONS



SIDE VIEW



REAR VIEW

NOTE: DIMENSIONS ARE NOMINAL AND INTENDED FOR SITE PLANNING USE ONLY.

F20D

FIGURE 28. DESK MOUNT